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DARPA/DSRC Workshop
October 5, 2000

INFORMATION DIRECTORATE

MIXED TECHNOLOGY SYSTEM REQUIREMENTS

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Overview

- Information Directorate Technology Focus
- Technical Directions
- Projected System Requirements Characteristics
- Suggestions For Mixed Technology CAD
- Conclusion

INFORMATION DIRECTORATE

Vision: Information Dominance for Aerospace Superiority

Objectives

Global Awareness:
Provide consistent, integrated battlespace information on demand, tailored to the needs of individual warfighters

Goals

- Automated exploitation tools 90% accuracy
- Fusion of information into single consistent operating picture providing situational awareness and impact assessment
- Affordable global information base supporting real-time exploitation and fusion

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Dynamic Planning & Execution:
Provide commanders with the ability to shape and control the pace and phasing of engagements, exploiting global awareness and global information exchange capabilities

- Capability for predictive planning and preemption, integrated force management and execution
- Capability for real time sensor to shooter operations
- Collaborative, distributed real-time mission planning, training& battlespace simulation

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Global Information Exchange:
Assure information anywhere, anytime, for any mission through adaptable and scaleable information systems

- Seamless collaborative workspaces
- X1000 increase in global comm to aircraft capability
- Continuous 24hr/day in transit visibility
- world-wide information on demand
- Information Warfare protect, detect, react
- Assured and survivable networking

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Joint Battlespace Infosphere Vision

Globally Interoperable Information "Space" that …

Aggregates, integrates, fuses, and disseminates tailored battlespace information to all echelons of a JTF

Links JTF sensors, systems & users together for unity of effort

Integrates legacy C2 resources

Decision-Quality Information

Focuses on Decision-Making

Enables Affordable Technology Refresh

Leverages Emerging Commercial Technologies

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Information Systems Needs

- Integrated information systems for consistent battlefield awareness
- Integrated GPS / Inertial measurement units for munitions, military platforms and personal navigation
- Digital data storage devices for volume / power / mass sensitive applications, i.e. spacecraft, distributed sensors, portable battlefield decision aids, unmanned air vehicles, etc
- Integrated RF Tags for asset tracking and for environmental / security surveillance
- Advanced architectures for voice / video / data communication

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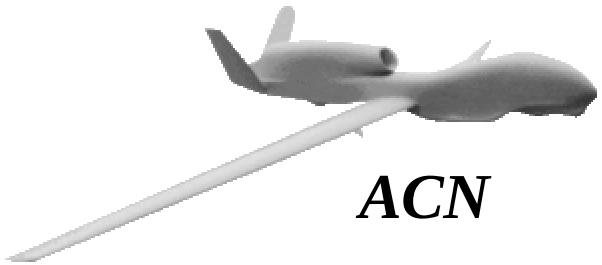
Global, Flexible Communications

Ground Forces

Airborne



ACN

- Revolutionary size, weight & power
  - Transceiver Requirements:
  - Compared wideband receivers in use today: 50X lighter, 50X smaller, 10X lower power
- Highly miniaturized, reconfigurable building blocks:
  - Single multi-band preselect filters
  - Frequency-agile nulling filters
    - Cosite interference, jammer resistance
  - Integrated frequency synthesis
  - Reconfigurable, low profile multi-band antennas
  - Adaptable matching power circuits
  - Radio frequency switches

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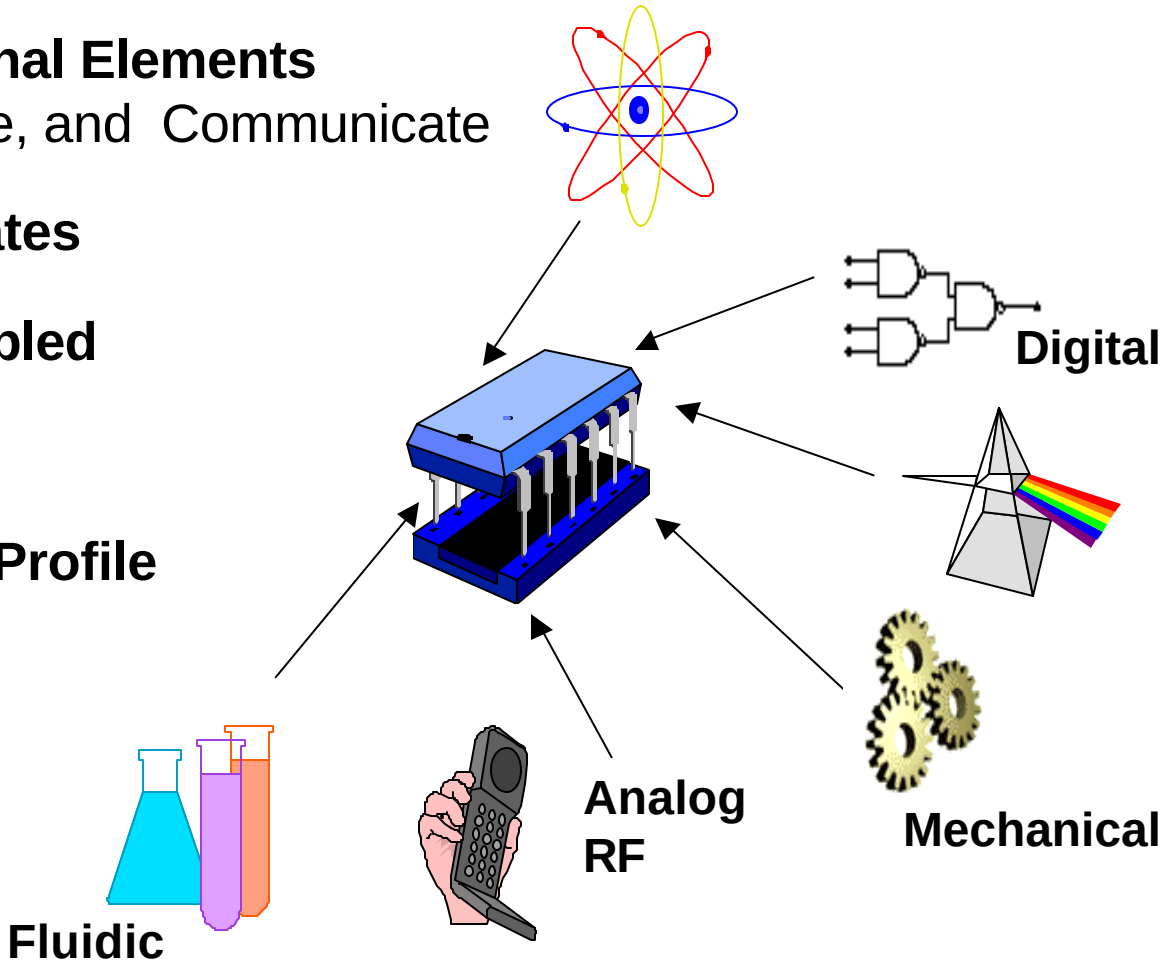
MIXED DOMAIN INFORMATION SYSTEMS

- **Future System Characteristics**
  - ✓ **Merging Functional Elements**
    Sense, Compute, and Communicate
  - ✓ **Common Substrates**
  - ✓ **Minimally Assembled**
  - ✓ **Low Cost**
  - ✓ **High Production Profile**



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MIXED SYSTEM CONCEPTS EXPLORATION / DEFINITION

- MATLAB Like Tools Drive Design Process
  - Tools Found Appropriate For Design Space Exploration
  - Extremely Effective: Analysis and Construction
  - Domain Integration and Analysis
- Quick What If Evaluation Required
- Automation Required
  - Bridge Concept to Implementations
  - Reduce Design Times
  - Establish Iterative Process Between Concept and Implementation

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SYSTEM ARCHITECTURAL DESIGN MIXED MODE SIMULATION

- VHDL-AMS
  - Disappointed Industry Roll out
  - Slowly Merging Digital, Analog, Spice Co-Simulation
  - Vendor Independent
  - Facilitates Multiple Energy Domains
  - Necessary Refine Gap Between Concept and Physical Level
    - Behavioral Assessment of Architectural Level Trade-offs
    - Hierarchical Interaction of Mixed Domain Systems
    - Assess the Effect of Parasitics on System Performance
- Future Directions

System Development Demonstrations to Establish Capability, Mature Technology and Exploit Current Work

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Synthesis

- Analog Synthesis Stalled
  - University Research Activity
  - Mature Research Concepts
  - Address Domain Interaction
  - Transition into Commercial CAD Tool Sets
- Complimentary Cell Libraries
  - Synthesis Driven Analog Cell Libraries
  - Automatic Scaling and Sizing

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MIXED TECHNOLOGY SUBSTRATE INTERACTIONS

- Quantify Parasitic Environment for Domain Interactions
  - Substrate Noise
    (For Example: Thermal, Brownian, Electromagnetic, RF, Switching)
- Experimental Structures Designed and Fabricated
  - Explore Multiple Design Isolation Techniques
  - Built-in, Calibrated, Noise Generators
- Define Isolation Techniques
  - Establish Design Guidelines
  - Predicative Model Assess Interactions/Isolation
- Address Analysis and Simulation of Multiple Substrates
  - Include Embedded Transitions Lines

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Conclusion

- Mixed Domain Design CAD Technology Required
  - Reduced Cost And Impact on System Development
- Air Force, DOD and Industry Have Common Mixed Technology Needs
  - Increased Integrated Functionality
  - Decreased Size, Weight, and Power
- Broad Technical Area
  - Carefully Scope and Select Specific Application Domains

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PHOTONICS AND MIXED SIGNAL COMPONENT TECHNOLOGY

5 OCT 00

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Sensors Directorate

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Rome NY

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Photonics Technology Overview

- Introduction
- The Need
- The Problems
- The Technology & Payoffs
- Component Level Research Programs
- Modeling & Integration
- Summary

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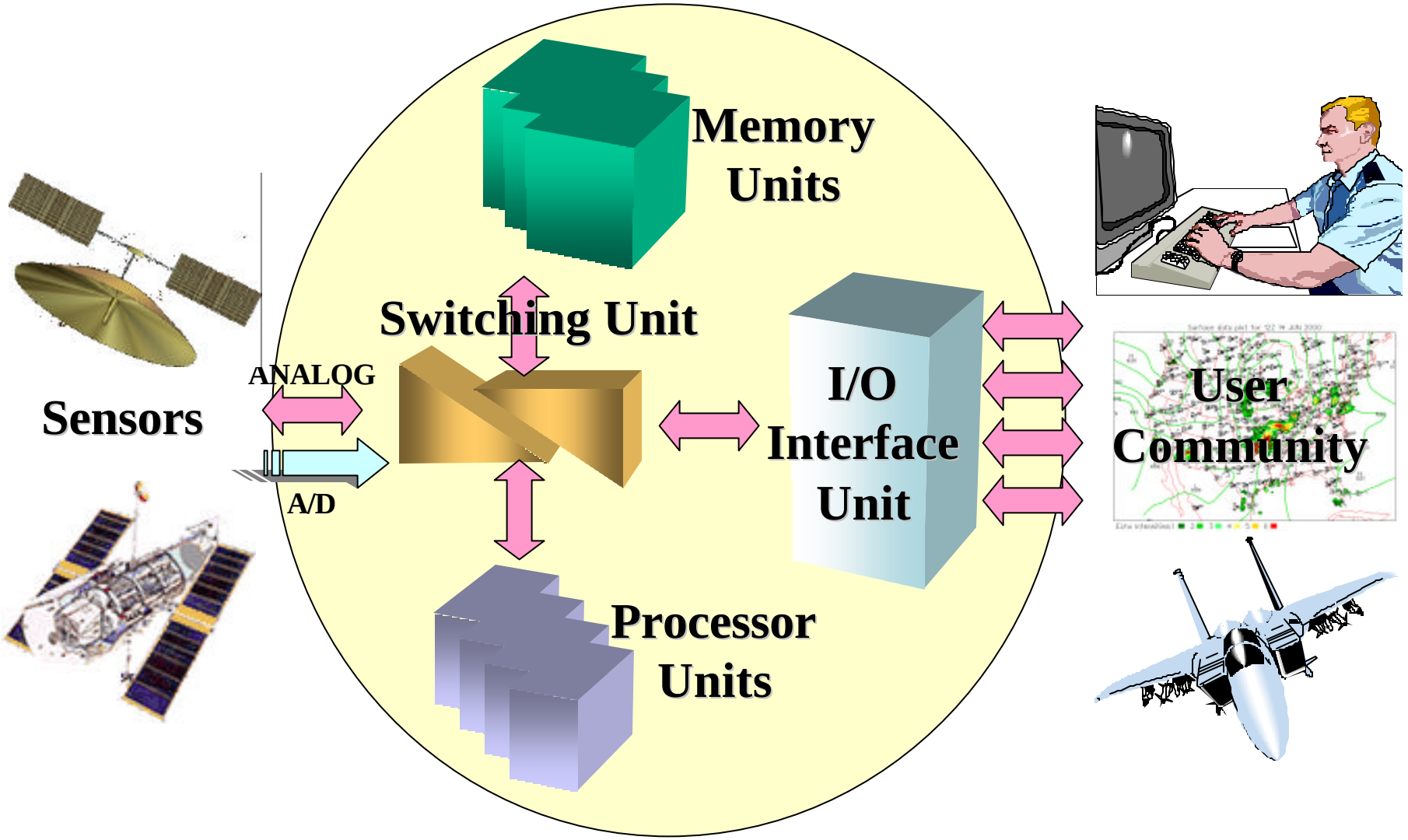
Information Chain

Sensor to Shooter



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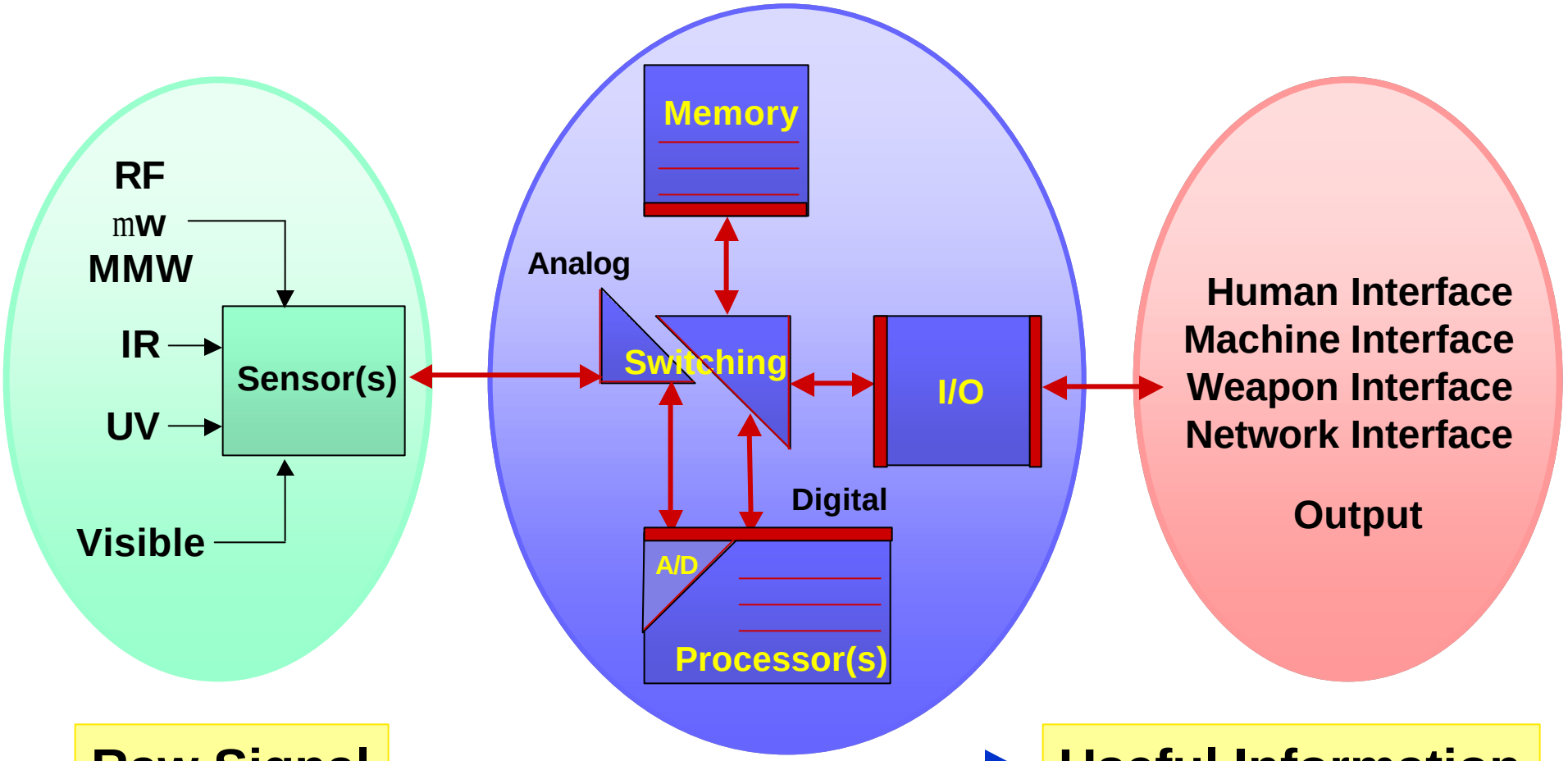
Platform Scale Networks

Platform Information System Functions



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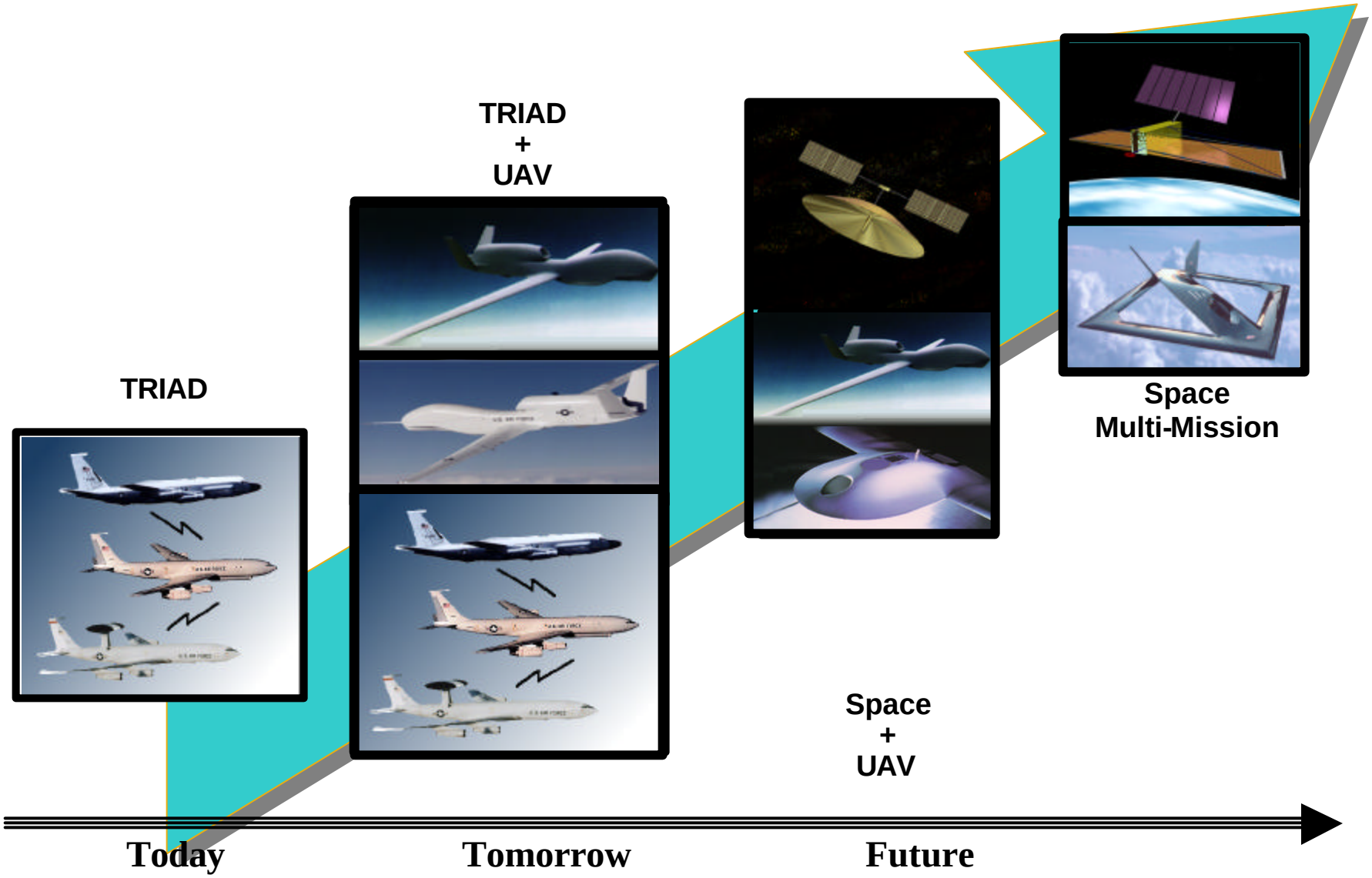
Global Multi-Mission Surveillance



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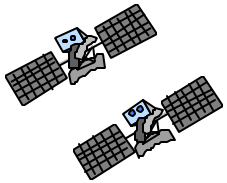
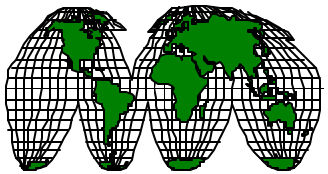
Opto-Electronics Program Goals



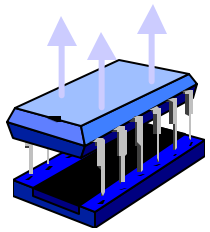
Merge the computational power of microelectronics, micromechanics, and optics to significantly lower system power, weight, and size, enabling a new generation of adaptable, real-time information processing micro-systems



- Bit rate independent I/O (all optical transport -> 10's Tbps)

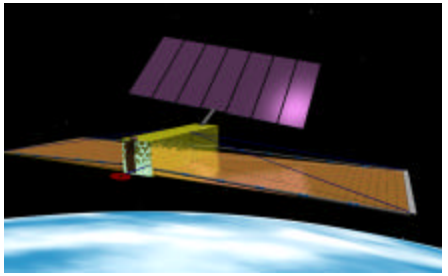
- Seamless communication for the war fighter

- Enabling > TFLOP Processing (switches & I/O reduction of volume*power by 2 to 3 orders of magnitude)



Adaptable & portable signal processors for small platforms

Portable onboard processing for the war fighter



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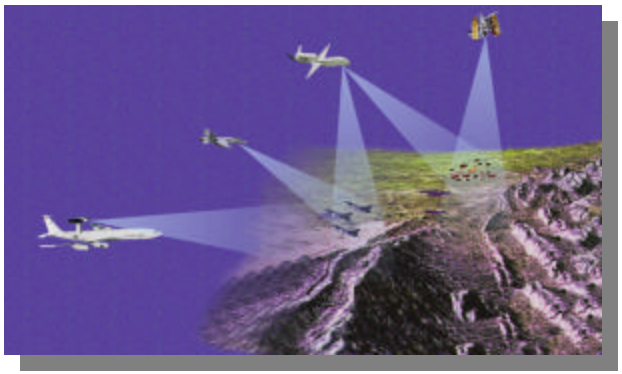
Photonics Technology

DTO Title: SE.36.01 Photonics for Control and Processing of Radio Frequency Signals

Objectives: Develop photonics technology to route, control, and process RF and microwave signals in military applications including photonic components and systems for control of phased array antennas and distribution of RF signals.



Payoffs: The antenna beam control technology will result in >1,000X improvement in bandwidth capability for ISR sensors and substantial cost savings due to lighter, smaller (by a factor of 100), and less complex assemblies. Beam control provides antijam, wideband, multimode phased array antennas for such applications as GPS and UAVs. Photonics also enables the remoting of antennas and emitters over kilometer distances, whereas coaxial links are limited to a few hundred feet by inadequate frequency response and dispersion.

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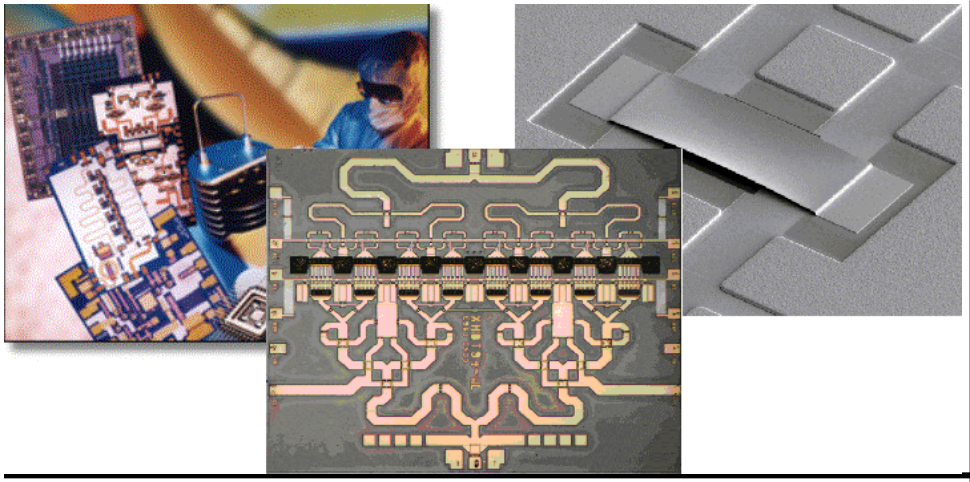
Pervasive/Enabling RF Technologies

Component Performance Enhancement



OBJECTIVE: To seek, assess, develop and demonstrate components with potential for 10x improvement in performance such as output power, increased dynamic range, increased signal handling capability, increased functionality, increased bandwidth, reduced RF loss and reduced conversion loss between RF, digital and optical domains

APPROACH:

- Pursue novel materials, devices and circuits
- Integrate photonics into RF front end
- Investigate novel radiating elements
- Push digital closer towards the radiating element

KEY DEVELOPMENT AREAS:

- RF Input Signal Handling Capability
- Differential LNA
- Wide bandgap materials and devices
- MEMS RF switches and time delay units
- Ultra wide bandwidth, low-profile elements
- RF and conversion loss between RF, digital and optical domains
- Output power density

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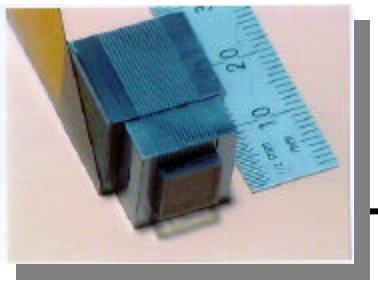
Photonics Technology

DTO Title: SE.35.01 Optical Processing and Memory

Objectives: Develop radically new optical concepts to achieve data storage of terabit to petabit (10**12-10**15) per cubic centimeter with nanosecond access times and optical interconnect technologies that provide terabit-per-second throughput between chips, boards, and processors. The goal is to achieve tera-operations-per-second processing in a massively parallel optoelectronic processor that is small in size and low in power consumption.



Payoffs: High-speed signal processing and information storage needs are driven by the operational realities of increasing jammer densities against C4I assets, low-observable target surveillance, and the requirement to manage large intelligence databases. Performance limits of conventional electronic approaches to air and ground surveillance are stressed by low-observable threats, sophisticated electronic countermeasures, increased target densities, and complexity of the modern battlefield, all of which make high-processing speeds essential. Hybrid or all-optical techniques provide solutions to the processing bottleneck at reasonable levels of cost, power, and volume.

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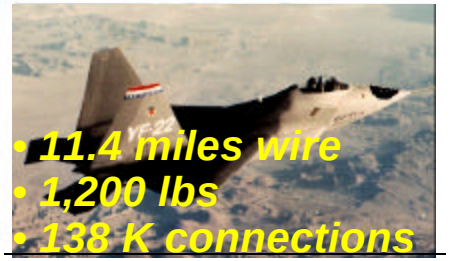
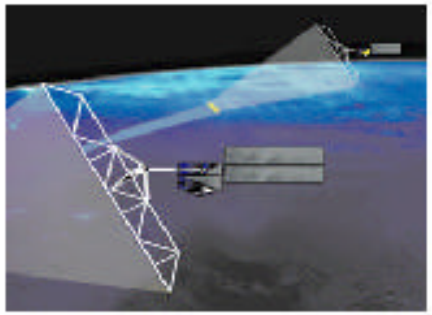
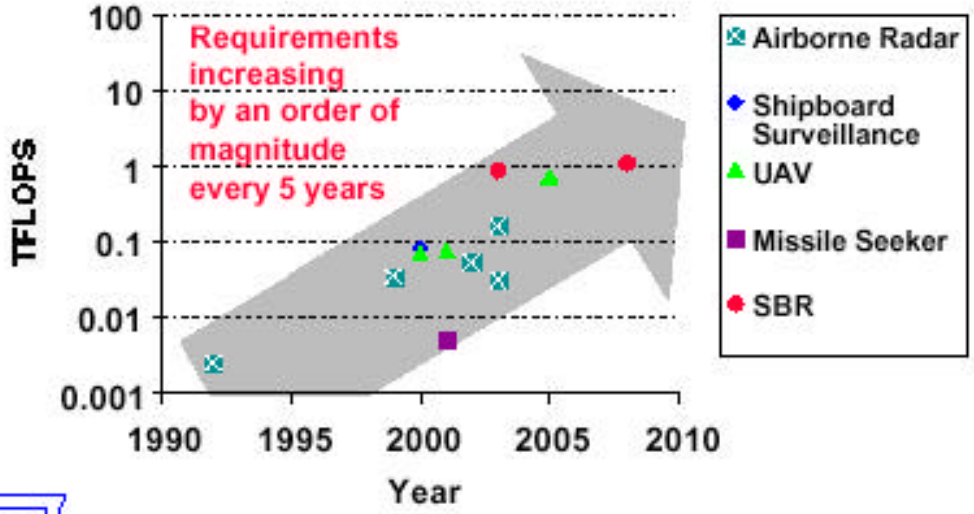
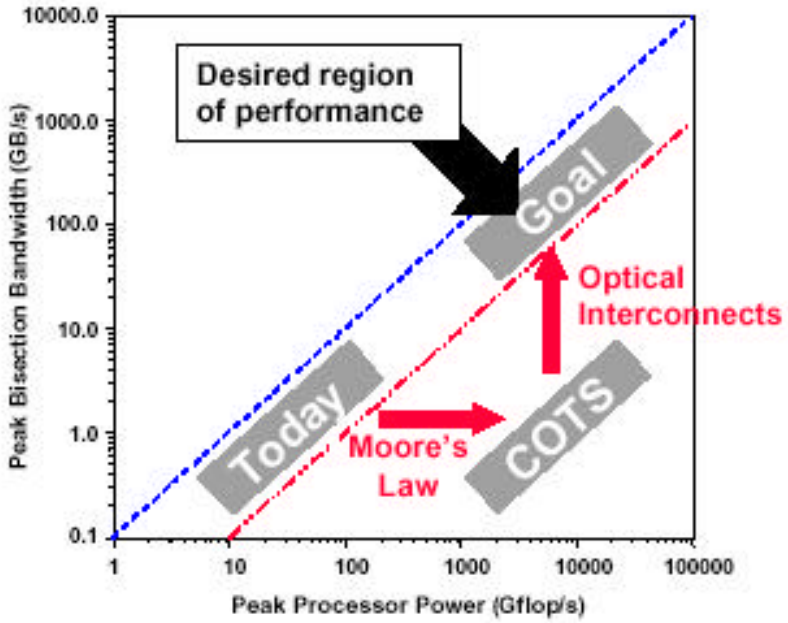
Real-Time Embedded Signal Processing









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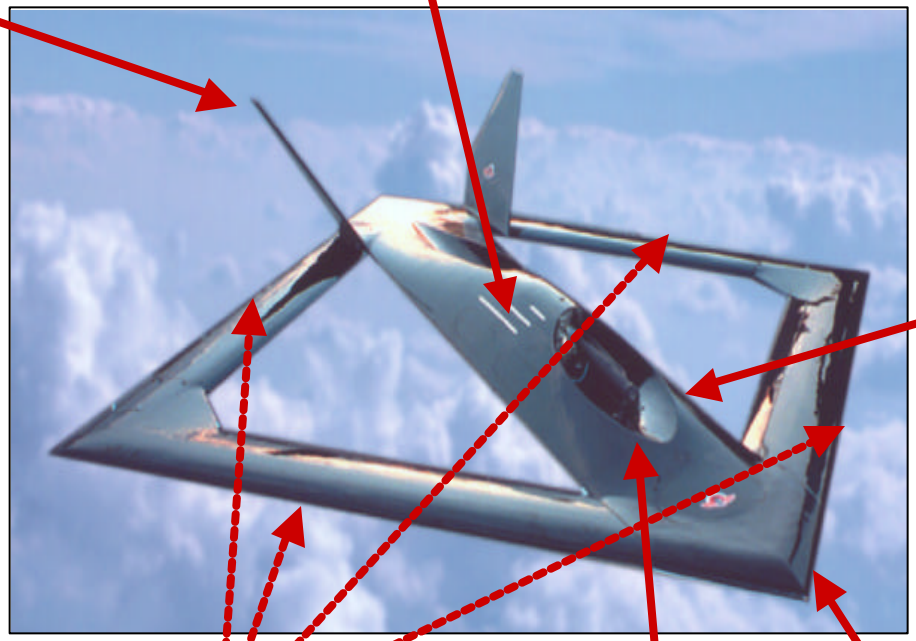
SensorCraft
Photonics Applications



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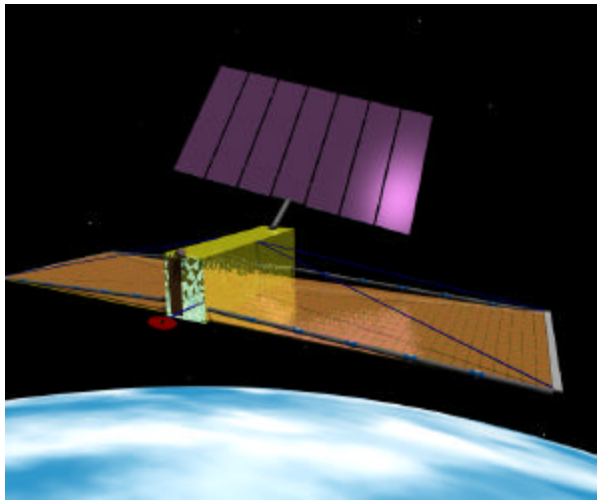
Space Based Radar (SBR)

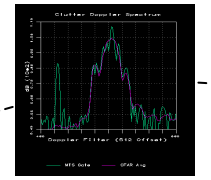
We Need the Ability to….

Detect and track targets of military interest in the theater of operations and around the world

- **Undeniable, All Weather Surveillance**
  - **Ground Moving Target Indication (GMTI)**
  - **Airborne Moving Target Indication (AMTI)**
- **Near Real Time**
- **Rapid Global Revisit**

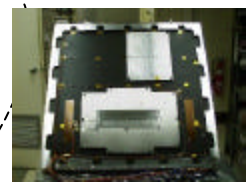


Phased Array SBR Satellite Concept



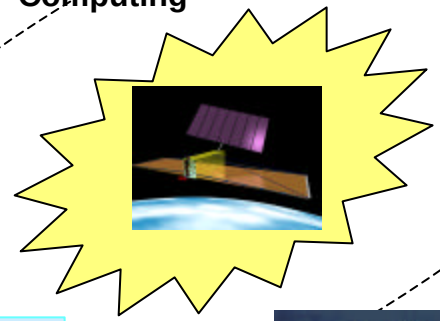
Radar Processing & Phenomenology/Modeling

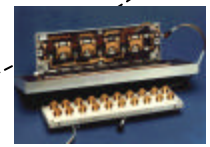
Computing



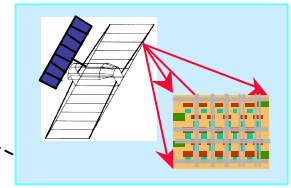
Adv Materials for Thermal Mgt, Radar, Power, Structures

Power





Light, Cheap Antenna RF Components



Large, Light Antenna Structure

THE WAY AHEAD: Affordable Satellite Architectures with key attributes of:

- **Very large, lightweight antennas**
- **Low cost, high efficiency RF components**
- **Low mass, high efficiency power sources**
- **Improved space computers & processing**

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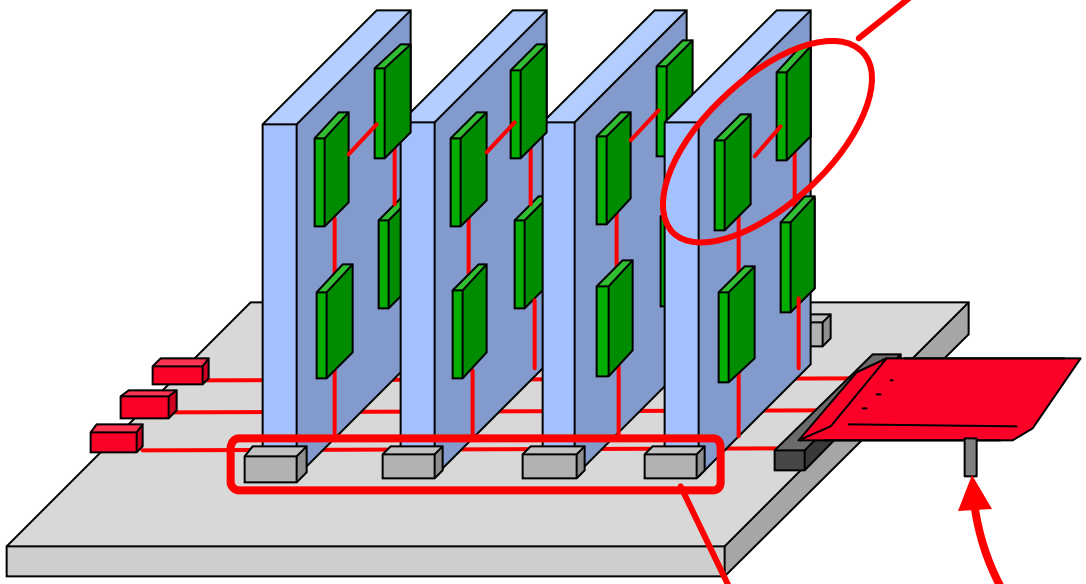
Electrical Interconnect Multi-Level Problem



Chip-to-Chip communication is bandwidth-limited

Incoming data rate ~ > Gbs/s

Communication at the backplane << Gb/s

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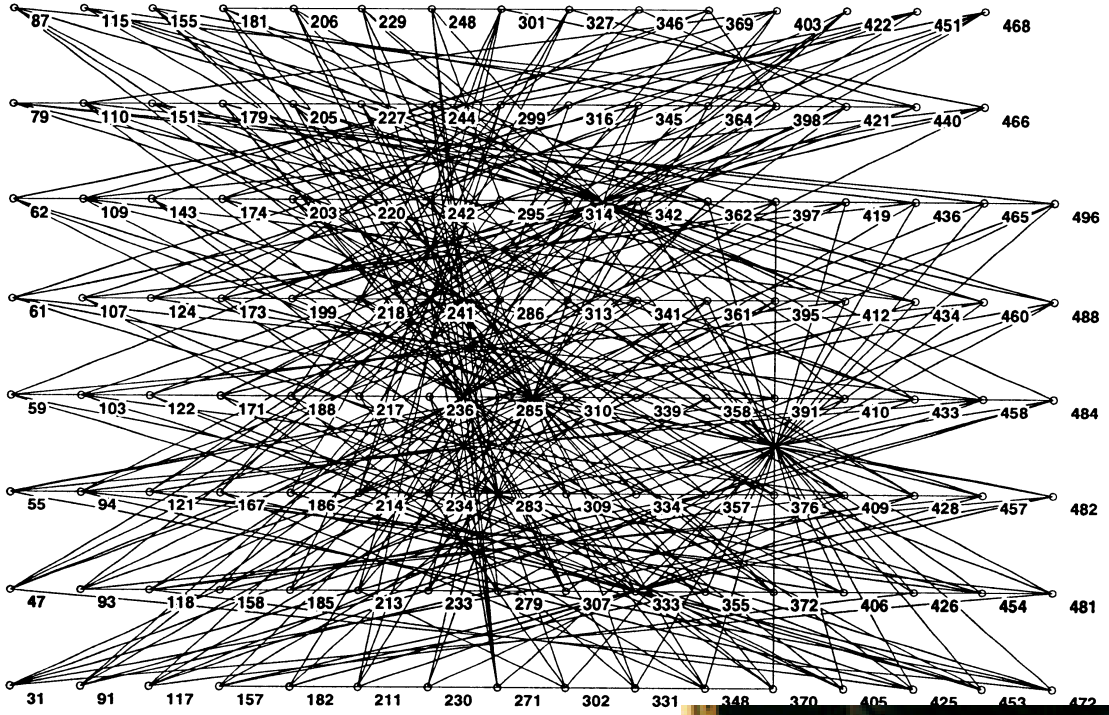
Electrical Interconnect Problem

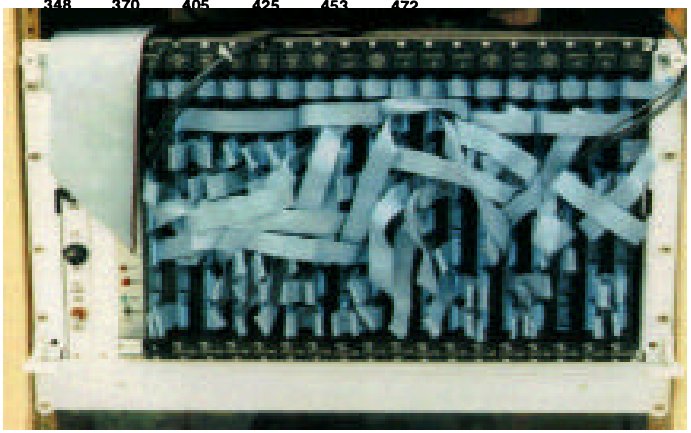
Example of 5-Degree Odd-Graph Interconnect Topology



Electrical Implementation Impractical Due to Contention, Latency, and Physical Restrictions

16 processor cards, each populated with 8 processing nodes, accessing a computer backplane

Current Aircraft Multiprocessor Backplane



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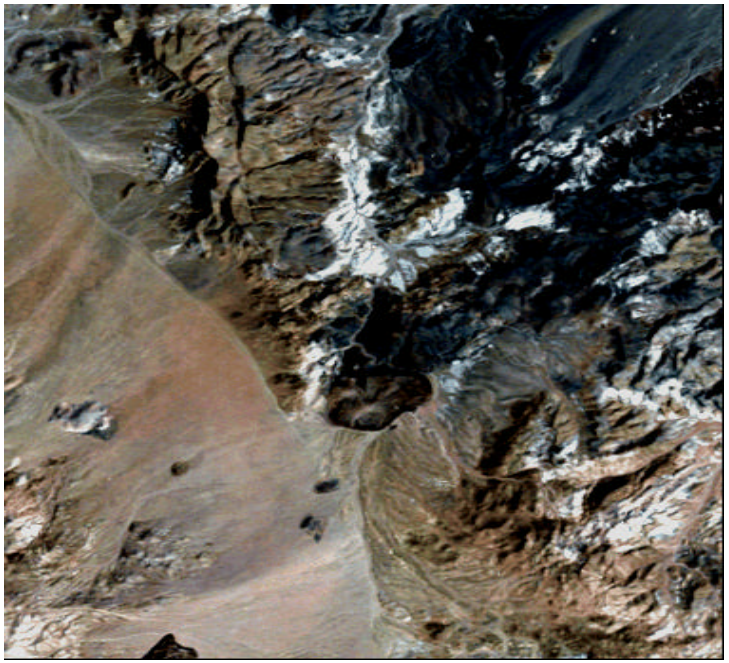
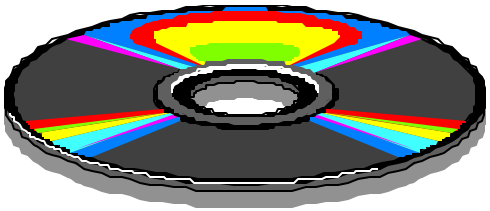
Opto-Electronics Terabit Communications Requirements

100 miles



100 miles

(1 ft resolution x 10 bits)



2.8 Terabit

Communication Rate	Time for 2.8 Terabit
• (T3 - 46 Mbps)	25 hours
• (OC48 - 2.5 Gbps)	15 minutes
• (Tbps)	2.8 seconds

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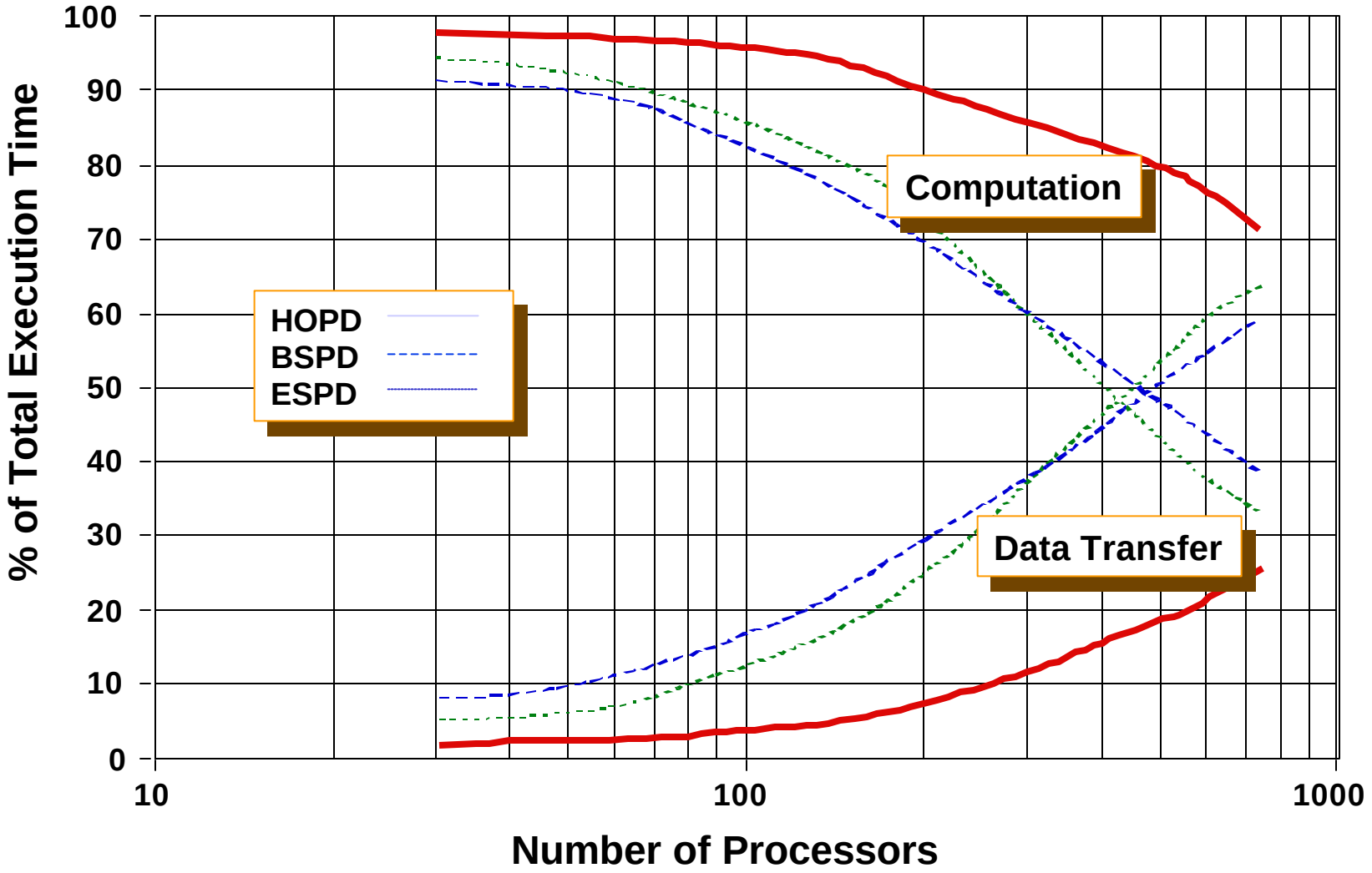
Data Communications Impact on Electronic Processor Interconnects

STAP Algorithm Models



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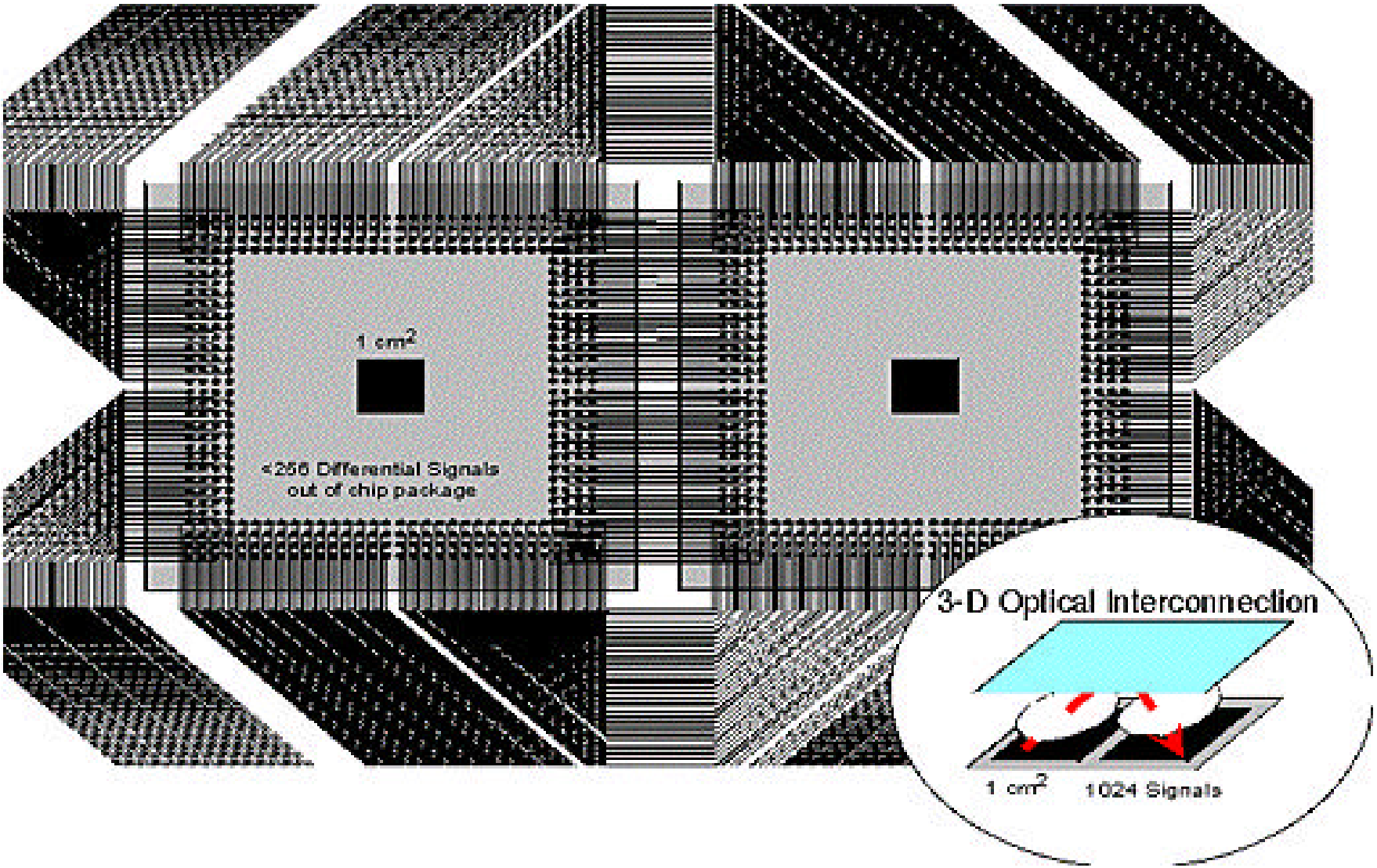
Planar Chip Interconnection Complexity



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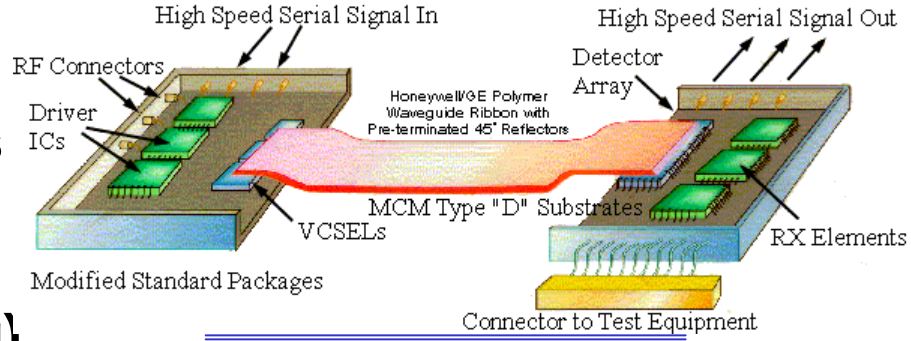
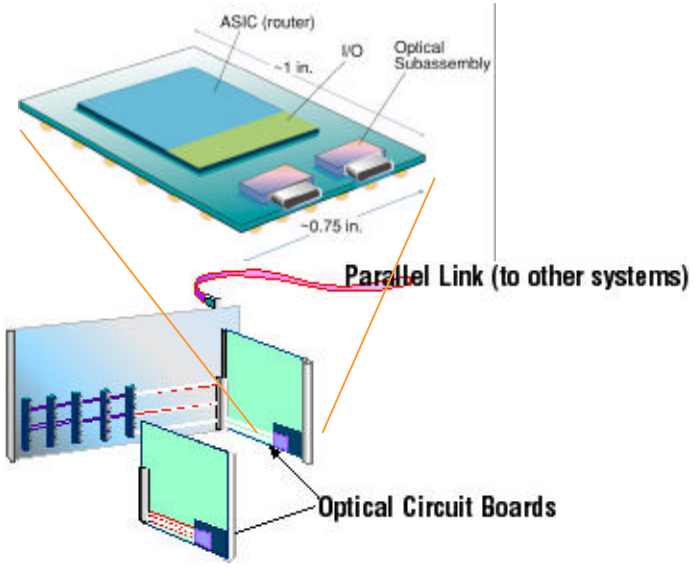
Photonic Systems Technology Research

AFRL/DARPA Research Partnership

Increase Processor Communication Fabric Bandwidth via System-Level Technology Development In:

- **Next Generation VCSEL Arrays**
- **Polymer Optical Waveguides**
- **Optical Interconnect Components**
- **Real-Time Performance and High Physical Density Demonstrations (Space-Time Adaptive Processing)**





Active Partnership/Co-Fund Programs

- *OMNET (network interconnects)*
- *FSOIA (free-space interconnects)*
- *VLSI Photonics (on-chip high bandwidth)*
- *PACT Optical A/D (high speed digital)*
- *RF Photonics (signal distribution)*
- *RFLICS (modulators & switches)*
- *AFRL O/E Inhouse Research (digital & analog)*
- *SBIRs, etc…….*

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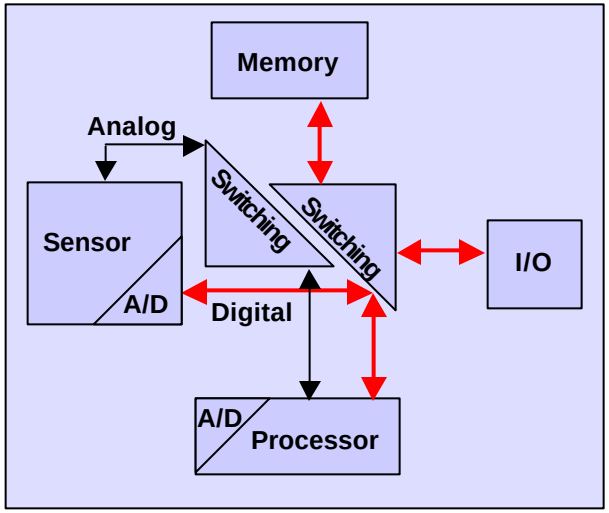
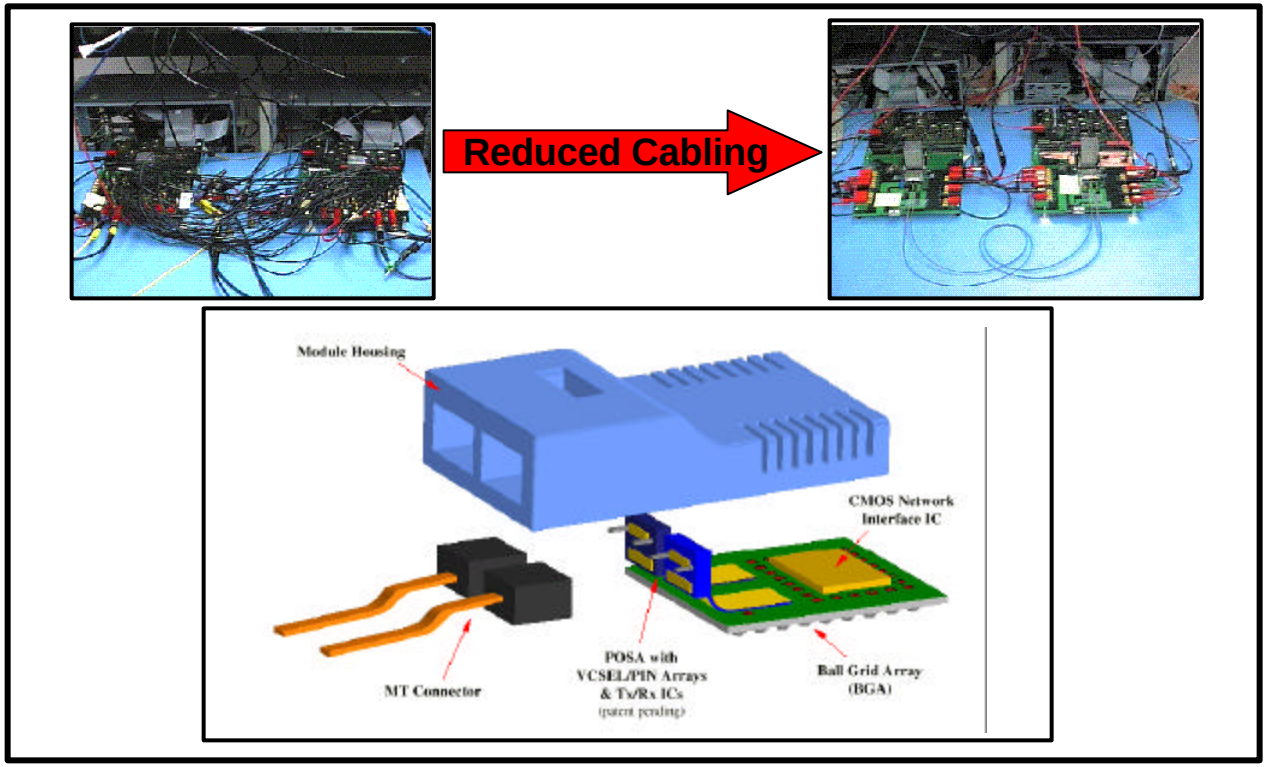
Optical Micro Networks

High Speed, High Density, Platform Size Optical Network

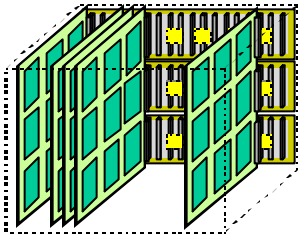


OMNET ↔



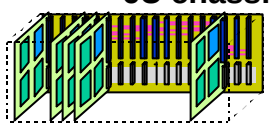
Military Impact

- On-board computationally intense processing
- High-speed, "future-proof" network technology supporting smart weapons



9U chassis

6U chassis



Platform Network Challenges:

- Crowded equipment bays
- Faster data transfer networks
- Network-CPU speed (Gb/s) divergence
- Bandwidth-Connector density limitations

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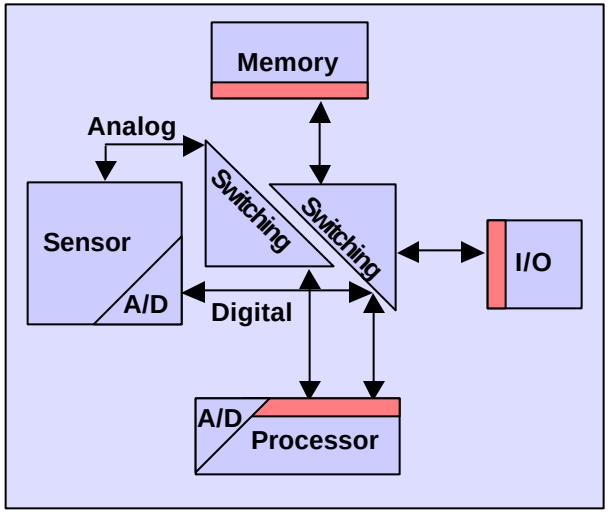
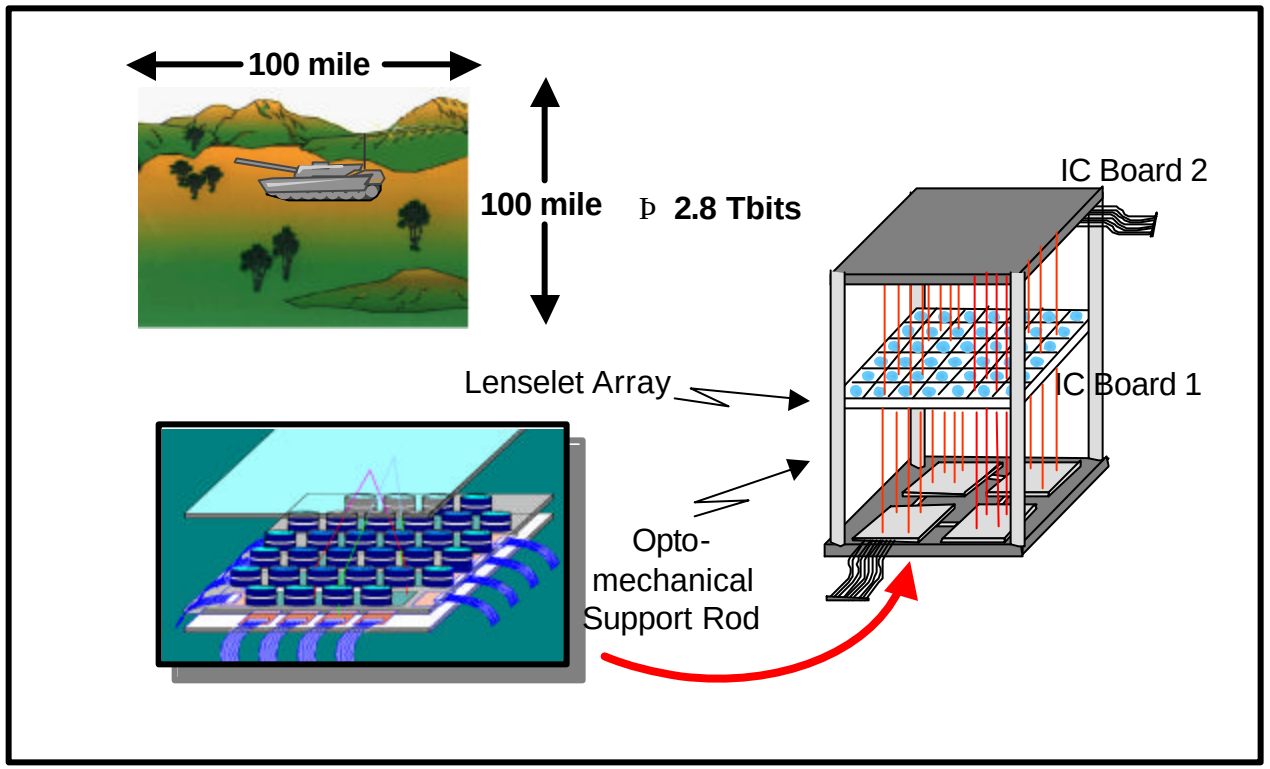
VLSI Photonics

High Density, Parallel, Short Distance Interconnects



VLSI-Photonics



Military Impact

- Real-time tasking of sensor platforms
- Dynamic targeting capability via compact, on-board TFLOP processing
- Access to portable Tbit memories
- Airborne Tbit communications node capability that can control and relay complex radar imagery and data

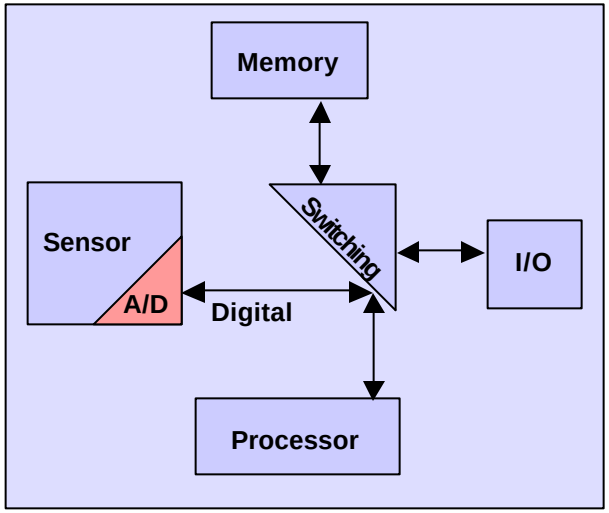
System Challenge of Imagery Processing:

– Imagery generates large amount of data requiring:

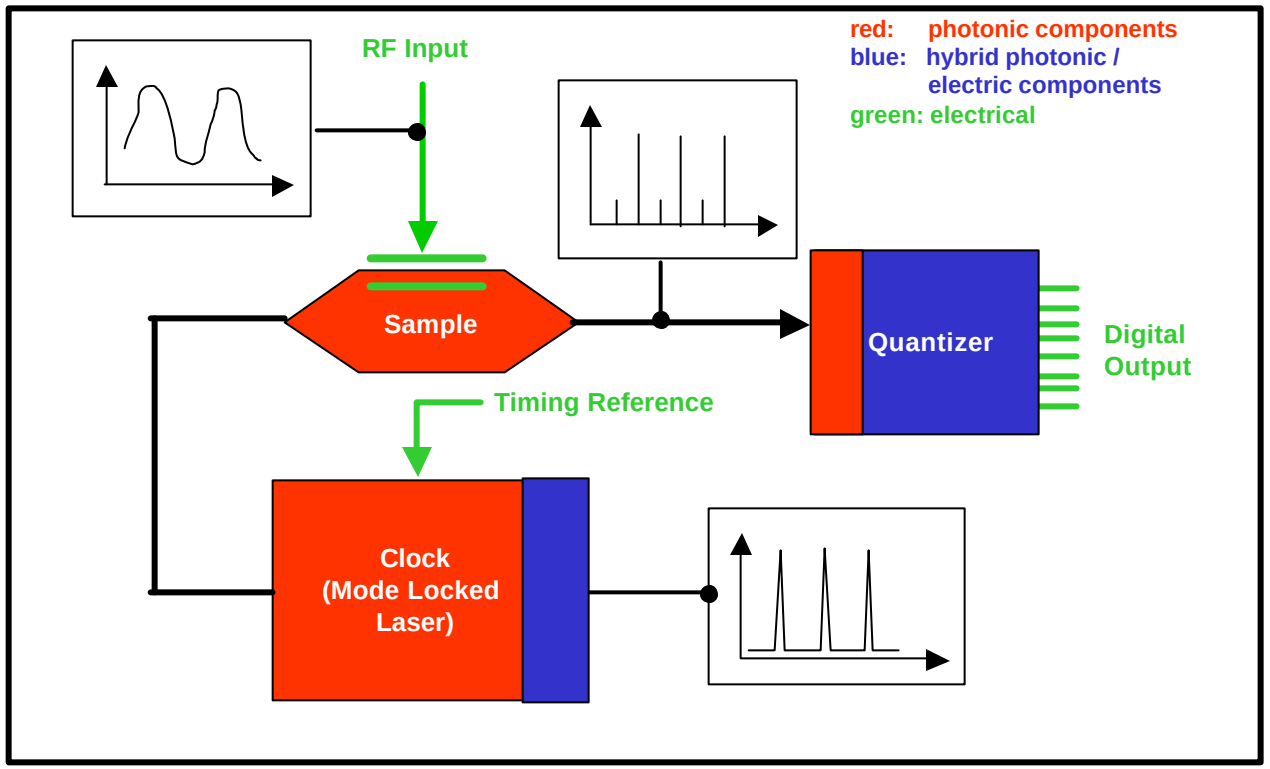
- Large I/O bandwidths
- Inter-chip access
- Rapid reconfiguration
- Accessing large memory capacities

Return

Photonic A/D Converter (PACT)



PACT



Military Impact:

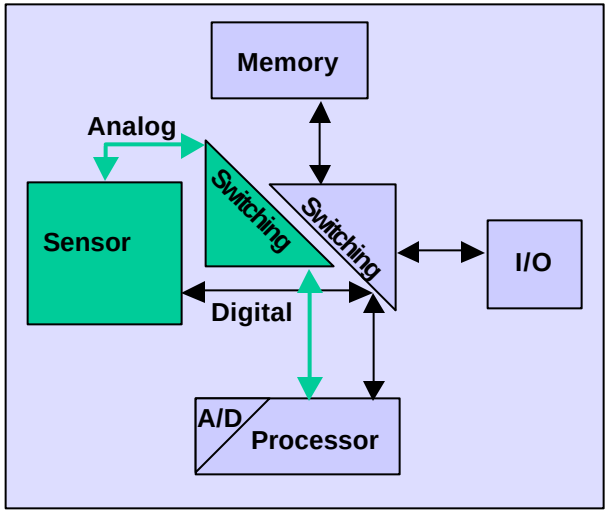
- Improved architectures and performance for radar, electronic warfare and communication systems.
- High resolution enhances jamming suppression, higher dynamic range and broader instantaneous bandwidth for target ID.

Challenges of Photonic A/D:

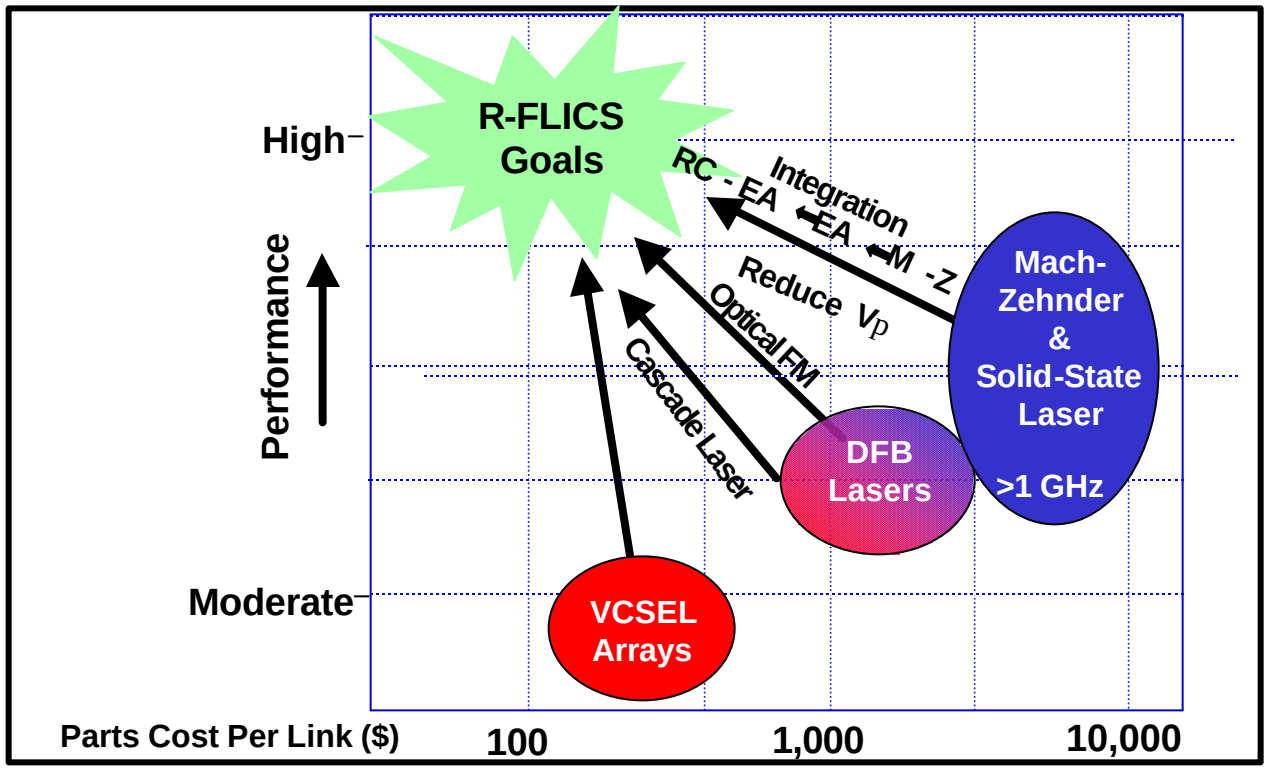
- High speed clocking
- Broadband sampling
- Signal interference
- Fiber vs waveguide dispersion

Return

RF Photonics
(RF-Lightwave Integrated Circuits)



RF Photonics ⟷



Military Impact:

- Expanded capabilities for critical RF systems; radar, EW and communication
- Enhanced RF signal processing via efficient, compact and lightweight very broadband components

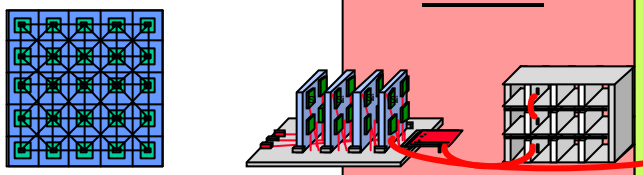
RF-Photonics Challenges:

- Low RIN Lasers
- Low Vp Modulator
- Efficient, High-Power Photodetectors
- RF Signal Processing OEICs

Return

Interconnect Frontier

Network Scale:	On Chip	Chip-to-Chip	LAN	Global
Program:		VLSI-P	OMNET	BIT
Photonic Technologies:	• Heterogeneous O/E Integration •Dense 2-D Arrays •Waveguide & Free Space •WDM	• GaAs based O/E • Si electronics • Freespace • 2-D arrays • DOE/VCSELs	• GaAs based O/E • VCSELs • mm Fiber/POF • Gb/s • Serial/parallel	• InP based O/E • SM-glass Fiber • Very high speed TDM • WDM



DARPA

1nm 1µm 1mm 1m 1km 1000km

VLSI Today (2000) — 325M Bits/cm^2

Projected Limits to CMOS (2015) — 17B Bits/cm^2

Transition to Quantum Devices

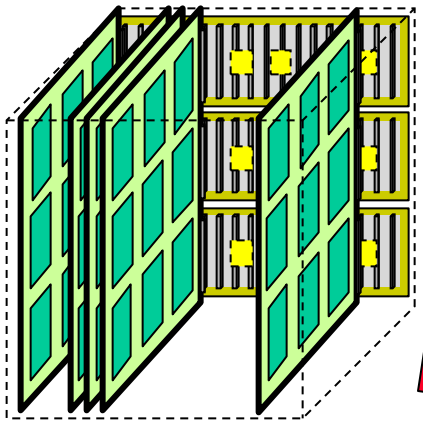
Atomic Scale — TBits/cm^2

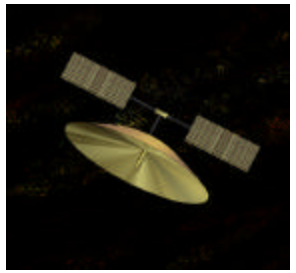
Return

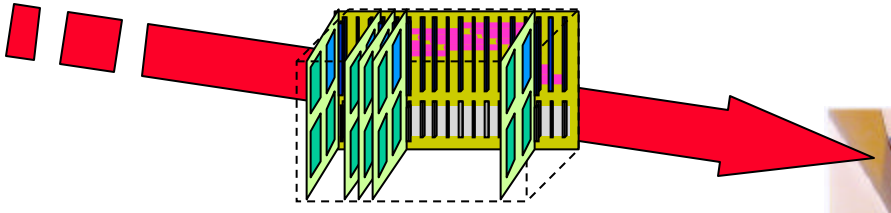
Advancements In Optical Interconnects

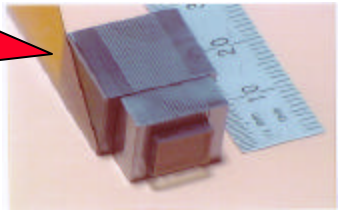
Overcomes the BW-density limits for metallic interconnects and enables Terahertz bandwidth networks for:

- **Sensor fusion**
- **Conformal/shared Apertures**
- **Low observables target detection**
- **Scalability for changing missions**
- **Smaller sensor platforms**





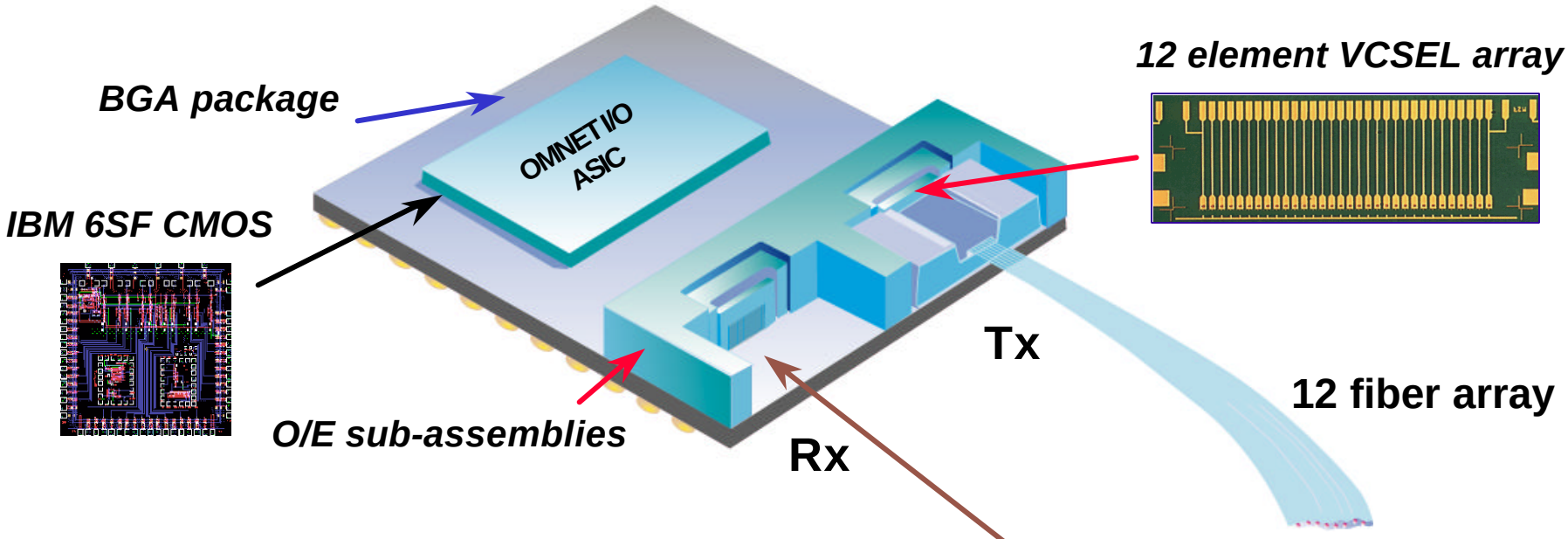




Reduced processor system size

Return

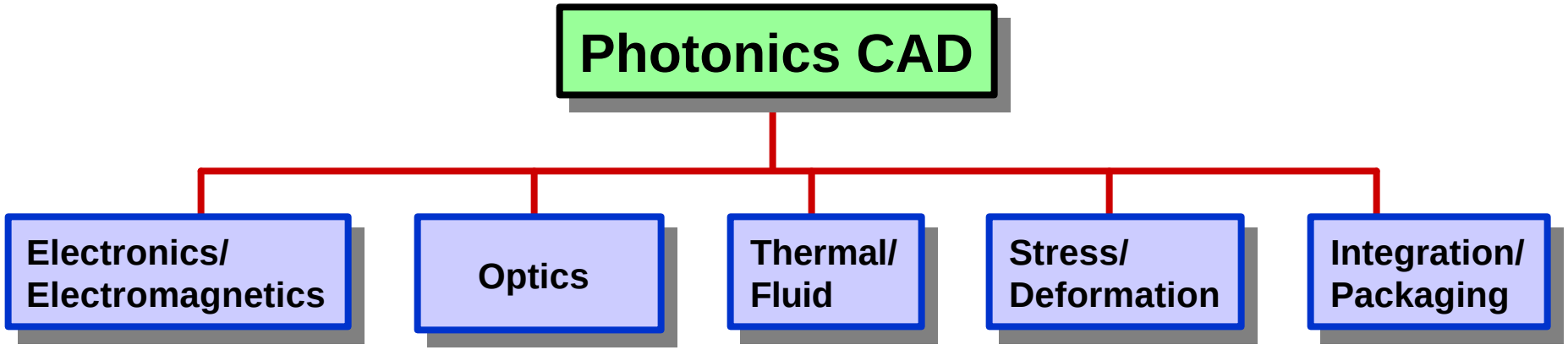
Integrated Opto-Electronic Parallel Data Transceiver



- ***Integrated CMOS I/O** buffer as standard cell to drive optics for ASIC; replaces > 2 separate Si bipolar ICs*
- *Integration of O/E interface with digital ASIC will **reduce cost, power, size***
- *Low Ith, high efficiency VCSEL array and low power, integrated receiver array (GaAs) **improves density, performance***
- ***>1.8 Gbytes/sec** aggregate Tx and Rx bandwidth from 12 channel array*

Return

Multi-Physics of Photonics CAD*



- Physics of Devices (VCSELs)
- Carrier Transport
- Lasing
- Self-heating
- Reduced (circuit) models for system design with:
  - SPICE
  - SABER
  - Chatoyant

- Beam propagation in fiber, in free space (geometrical, wave)
- Electromagnetics
- Coupling efficiency
- Lenses, mirrors
- Multiplexing, amplification, modulation

- Device heating (thermal crosstalk)
- Package cooling
- System cooling
- Thermal influence on optical properties
- Air damping of moving rotating optical devices

- Thermal stresses
- Vibration
- Tolerancing
- Optical alignment

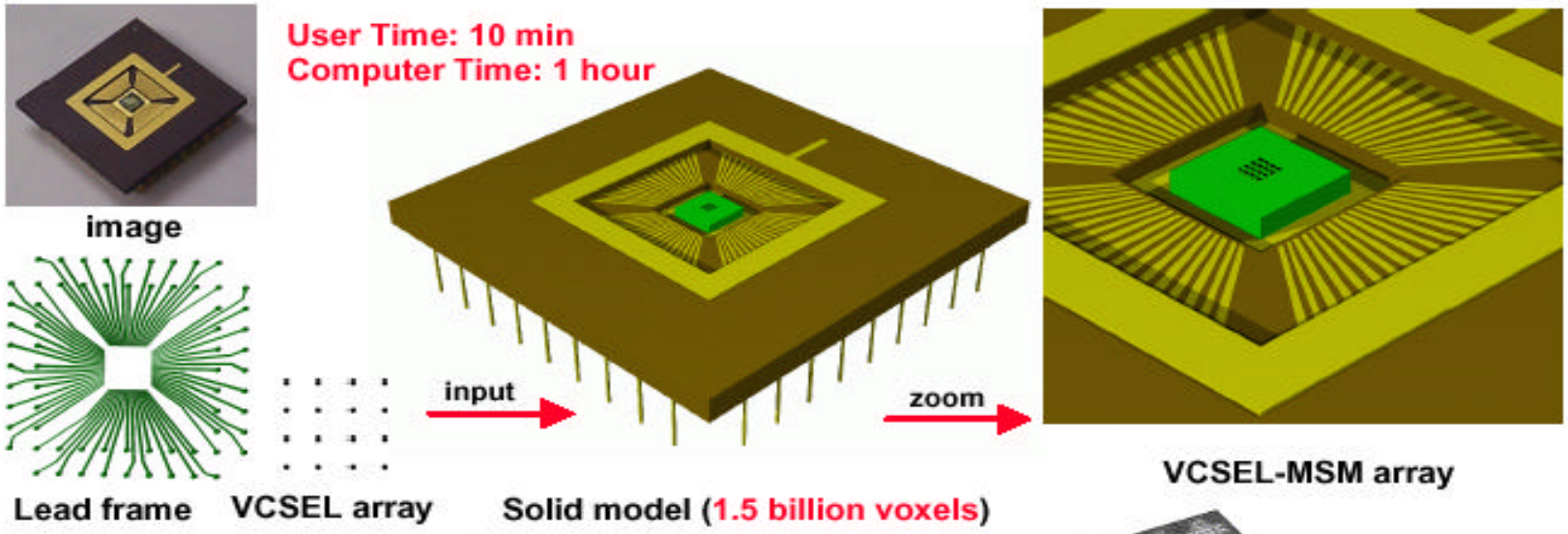
- System level simulation
- Mixed signal design
- Mechanical design
- Thermal cooling
- Fabrication, materials
- Multi-disciplinary coupling

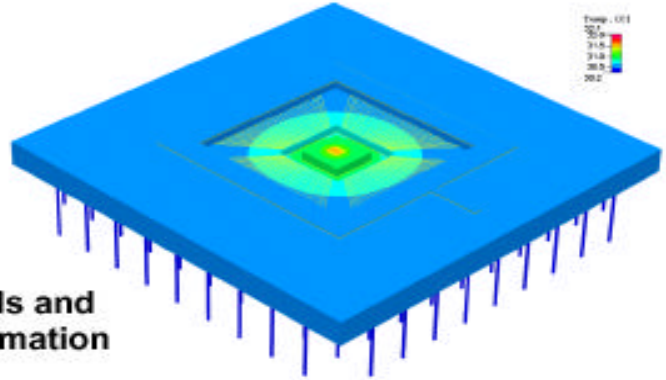
*CFDRC VLSI Photonics briefing to DARPA, Feb 00

Return

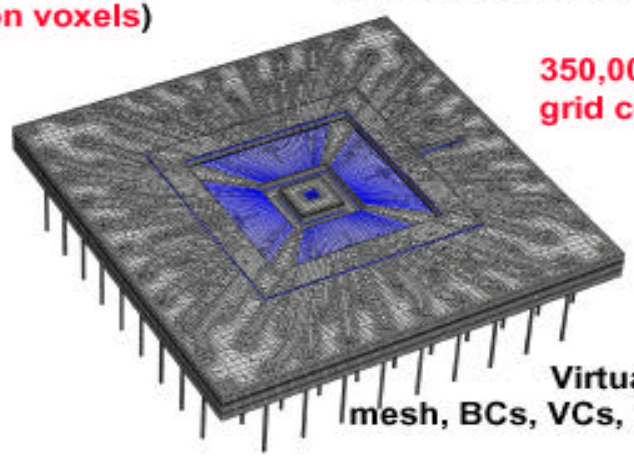
VCSEL Device and Package Model*

CFD-ACE+ Models of Honeywell VCSEL-MSM Array in 64-Pin PGA





Solution:
thermal fields and
stress/deformation



Virtual model:
mesh, BCs, VCs, materials

*CFDRC VLSI Photonics briefing to DARPA, Feb 00

Return

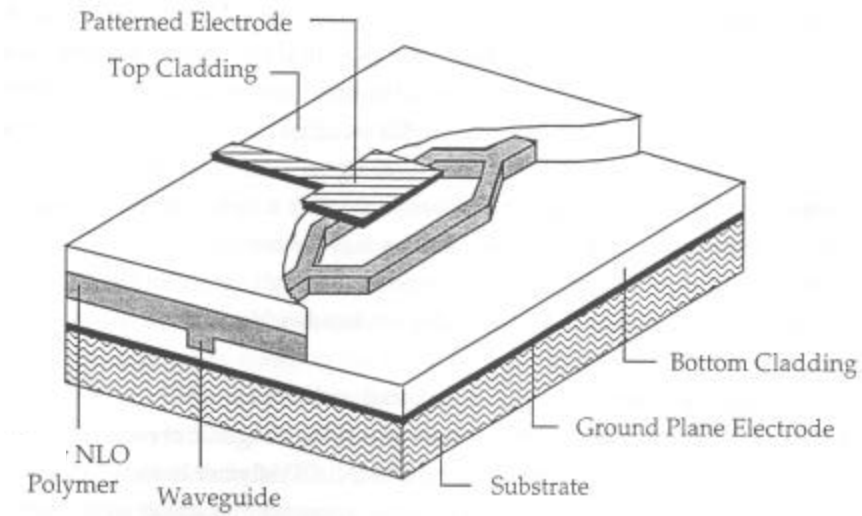
Designing a Mach-Zehnder Interferometric Polymer Modulator

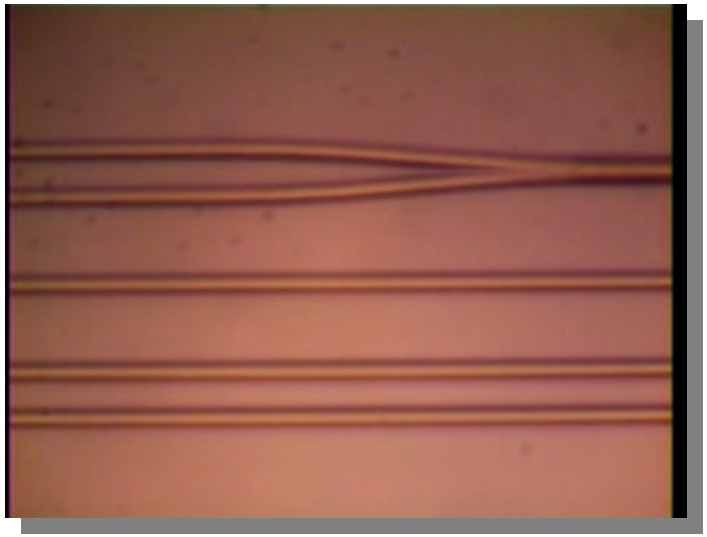
- Design/Simulate Optical Waveguides; Port to Layout CAD Package
- Design/Simulate Microwave Waveguide; Port to Layout CAD Package
- Draw/Align Optical and Microwave Structures to Make Layout for Mask Set

Optical Waveguide Design/Simulation

- BPM CAD - 2D or 2.5 D
- BEAM Prop - 2D or 2.5 D

Both based on Forward Beam Propagation Method



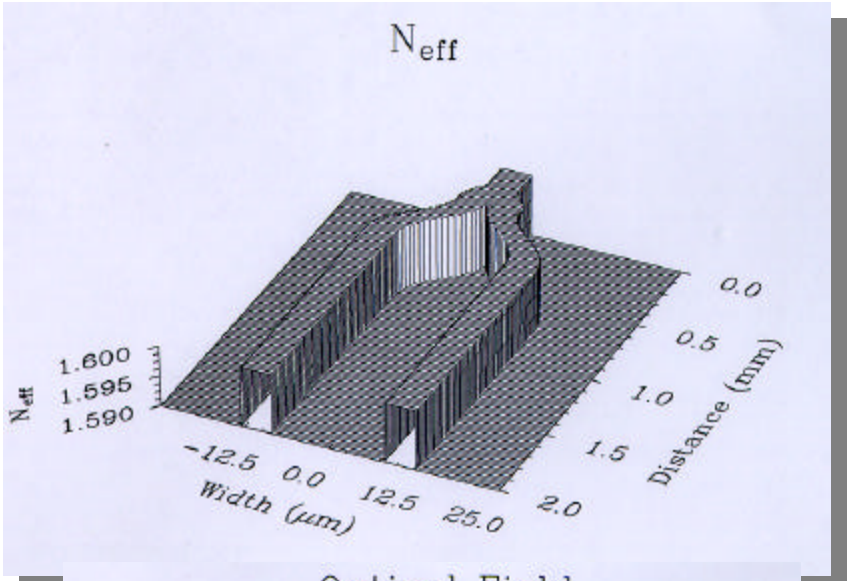


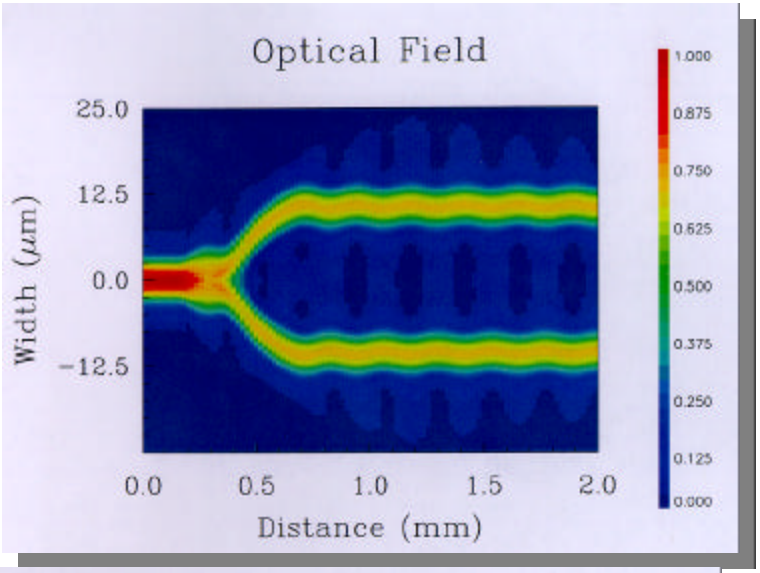
Microwave Waveguide Design/Simulation

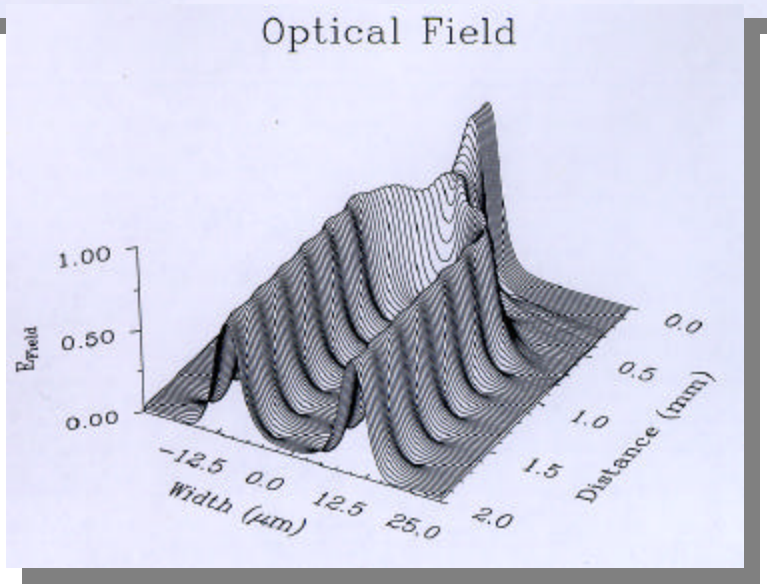
- HFSS (Ansoft Software Inc.)
- Ensemble (Ansoft Software Inc.)
- Serenade (Ansoft Software Inc.)
- Sonnet

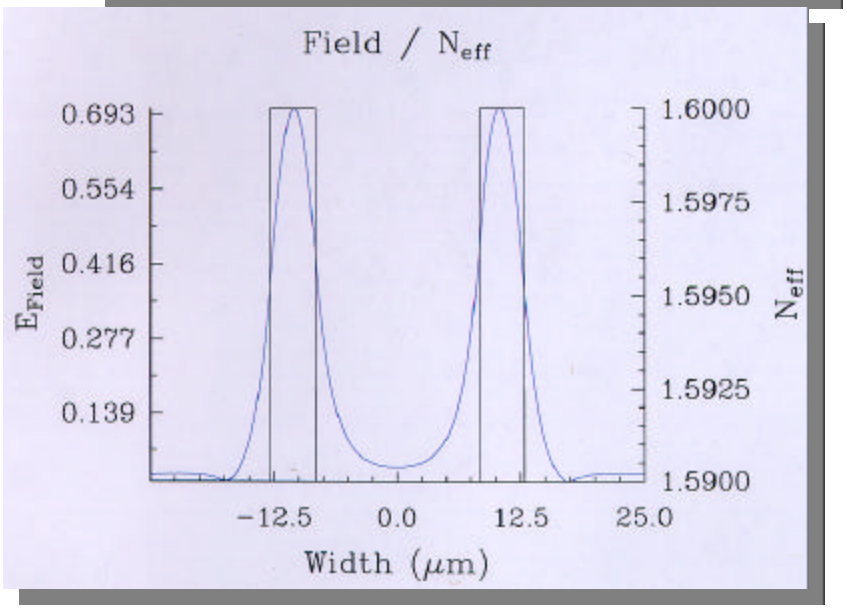
Return

Modeling an Optical Waveguide









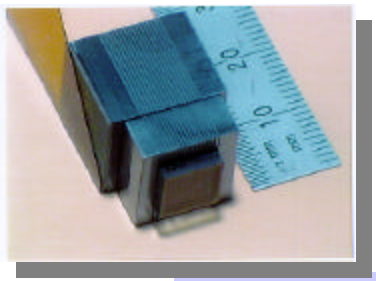
Return

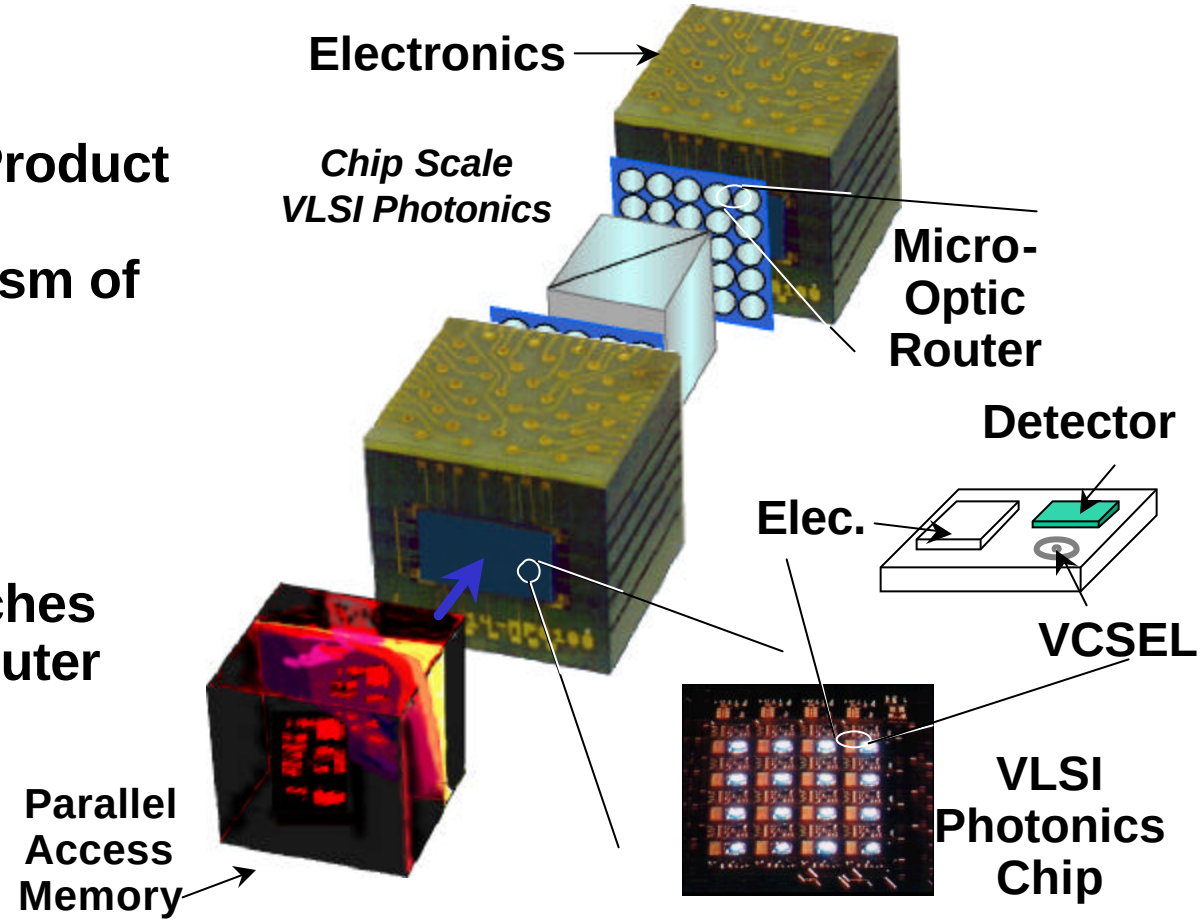
3D Opto-Electronic Signal Processor

Demonstrate 100-1000x Improvement in Speed•power•volume Product Exploiting Optics, VLSI Photonics and Parallelism of Optics Over Electrical Techniques

Applications:

- **Ultra Smart Sensors**
- **Fast Database Searches**
- **Portable Supercomputer**



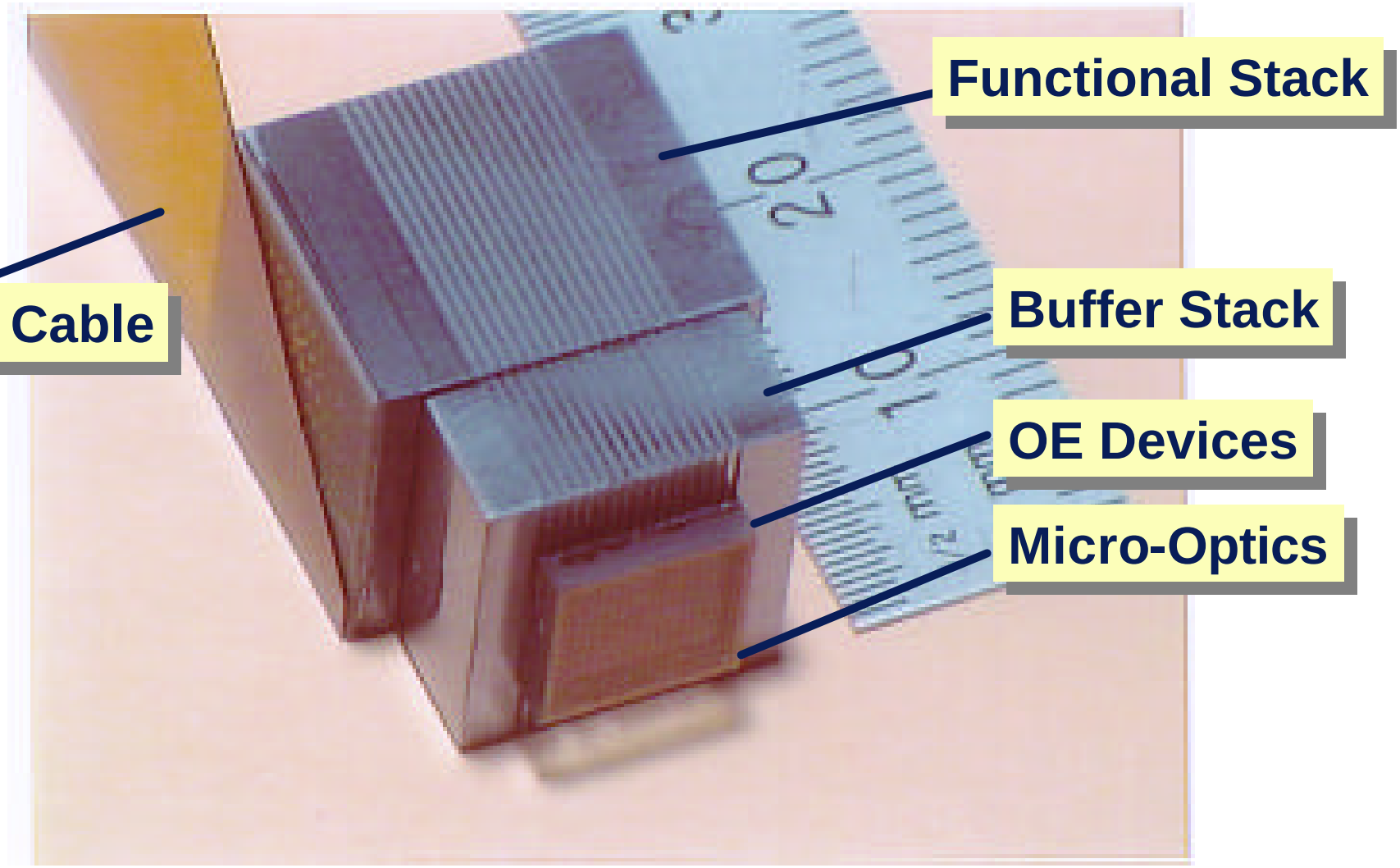


Example: Lateral System With 16x16 VCSEL/MSM Arrays Offer:

- **256 Gbits/sec Interconnects ; 100 W ; 15 cm^2 ; 45 cm^3**
- **6 kW/ $foot^2$; 60 kW/$foot^3$; 150 Tbits/s/ $foot^3$**

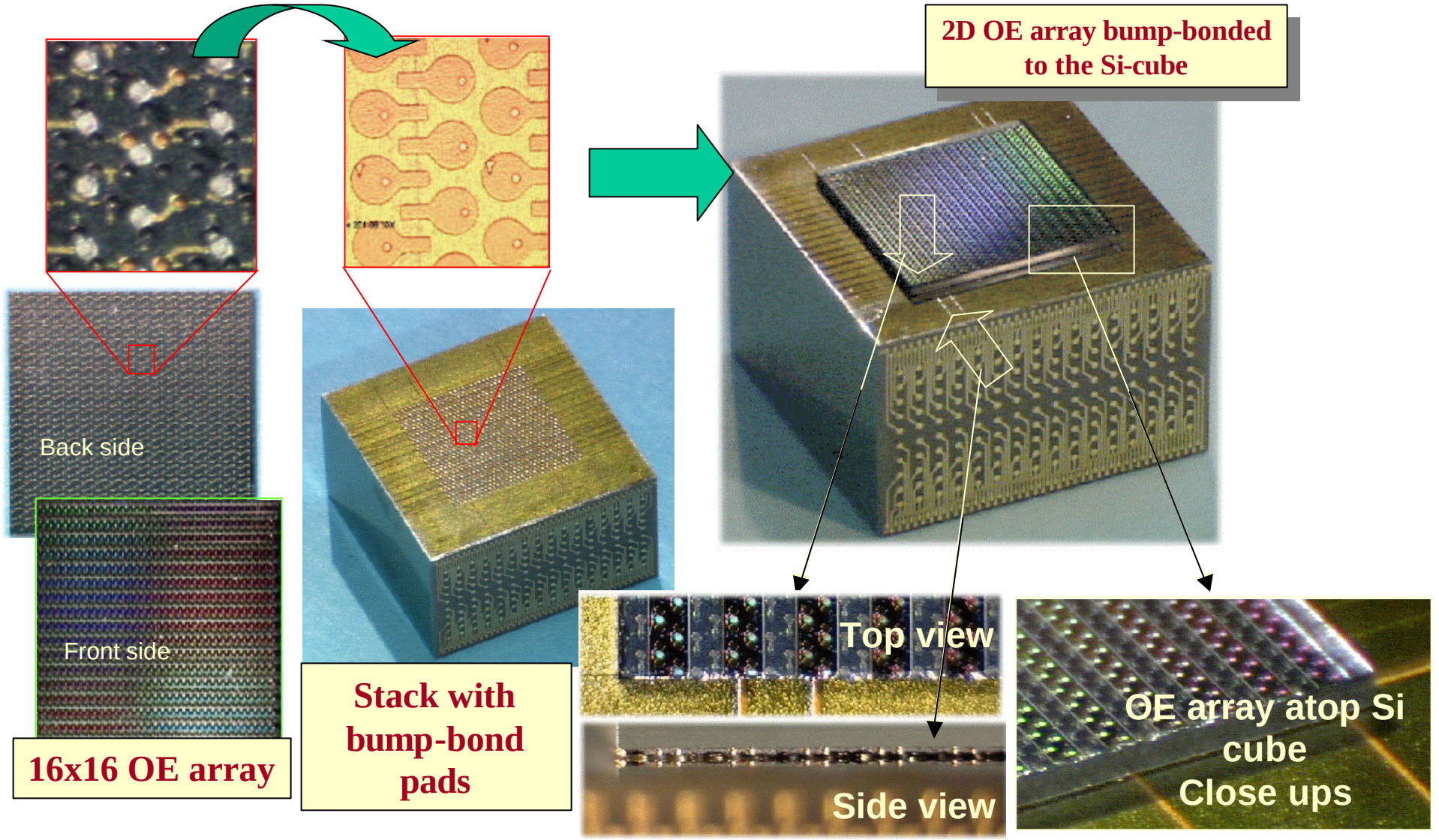
Return

3D-OESP Module



Return

3D-OESP Opto-Electronic Stacks

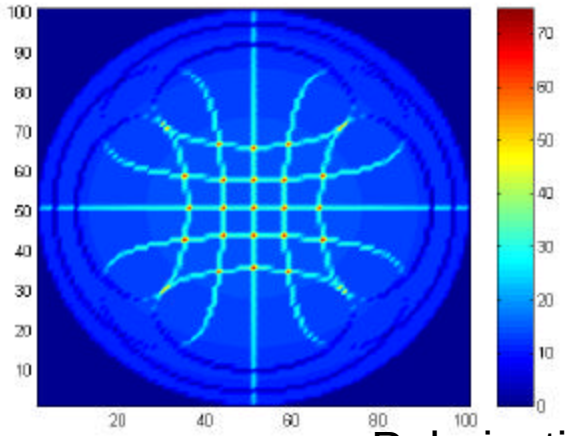


Return

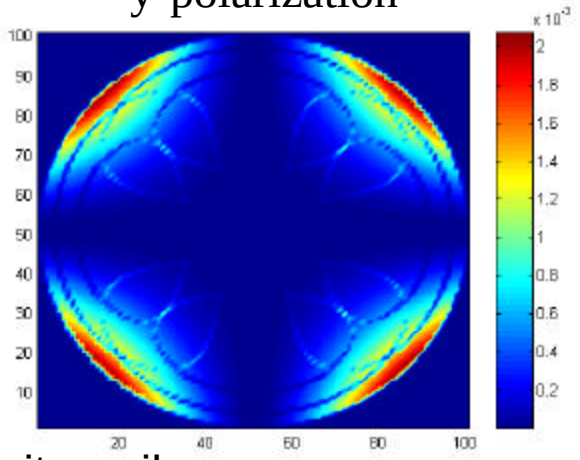
Accurate Modeling of Micro-Optics

Unexpected polarization effects observed from rigorous modeling techniques.

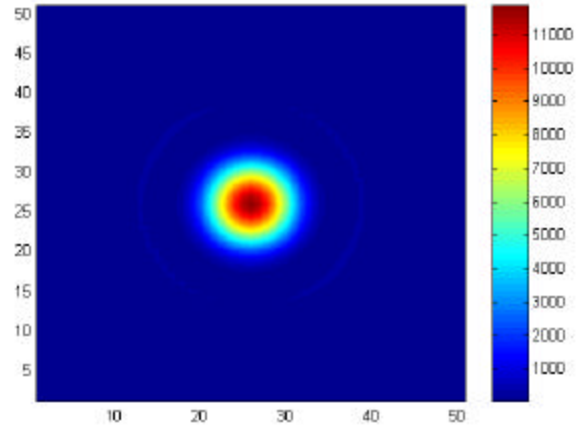
x-polarization

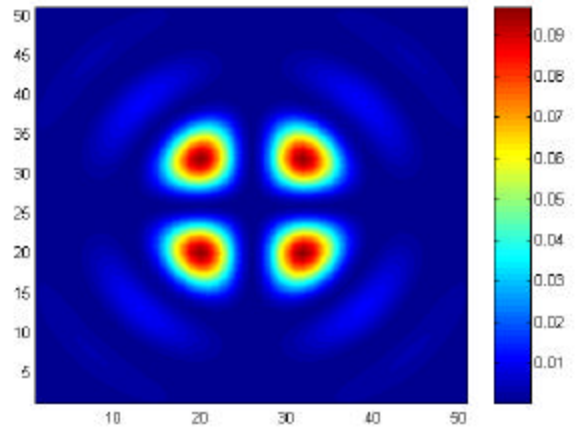


y-polarization



Polarization at lens exit pupil





Polarization at focal plane

UCSD (Fainman)

Return

Free-Space Opto-Electronic Modeling and Simulation

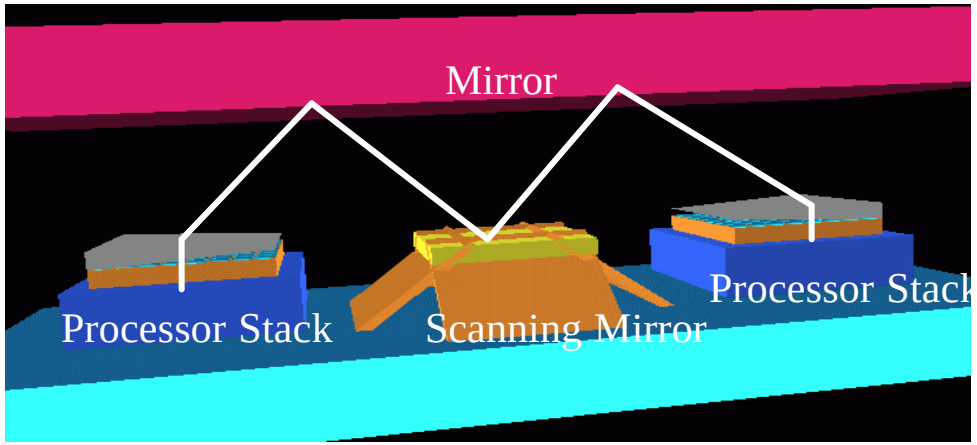
Goals:

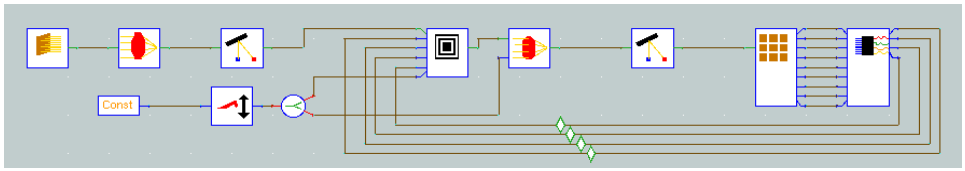
- Simulation and modeling of FSOI Systems in terms of BER, power consumption, mechanical misalignment, beam shape, noise margins, insertion loss, crosstalk, etc.
- Analyze design trade-offs without costly prototyping

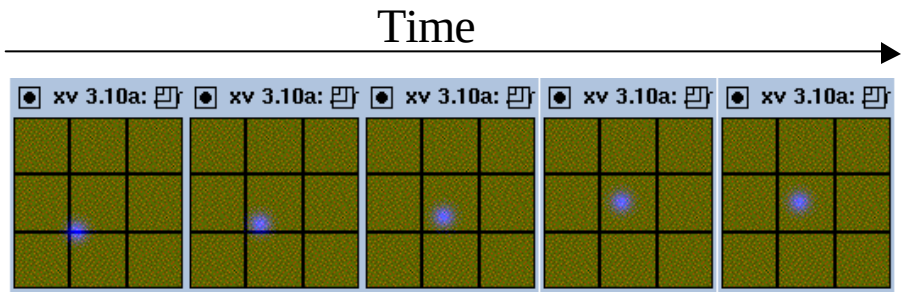
Recent Accomplishments:

- Chatoyant “alpha release” distributed for evaluation
- Optoelectronic and mechanical models based on piecewise linear solvers
- Incorporation of Rayleigh-Sommerfeld diffraction formulation for optical beam propagation
- New Java 3D GUI

Beam steering with scanning mirror



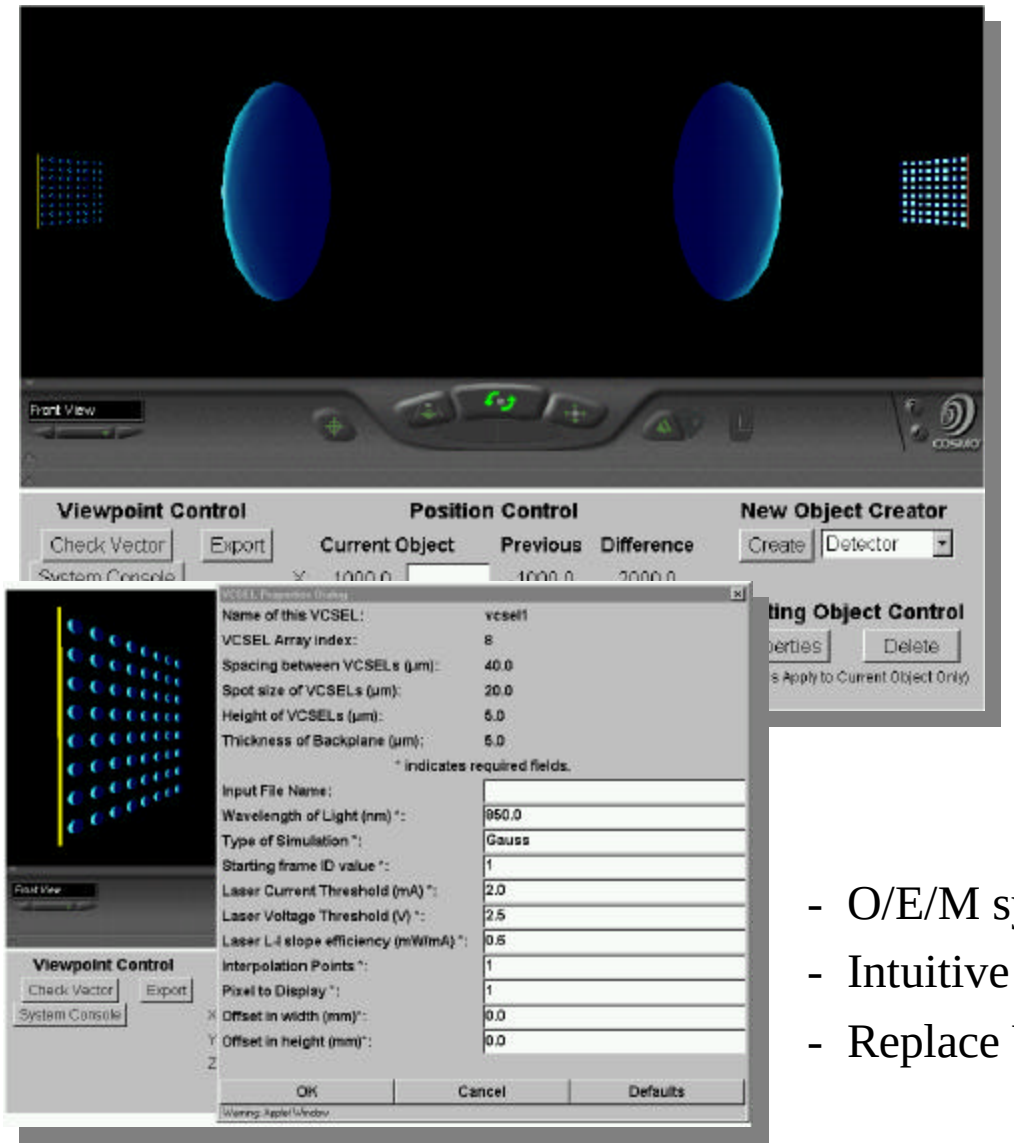


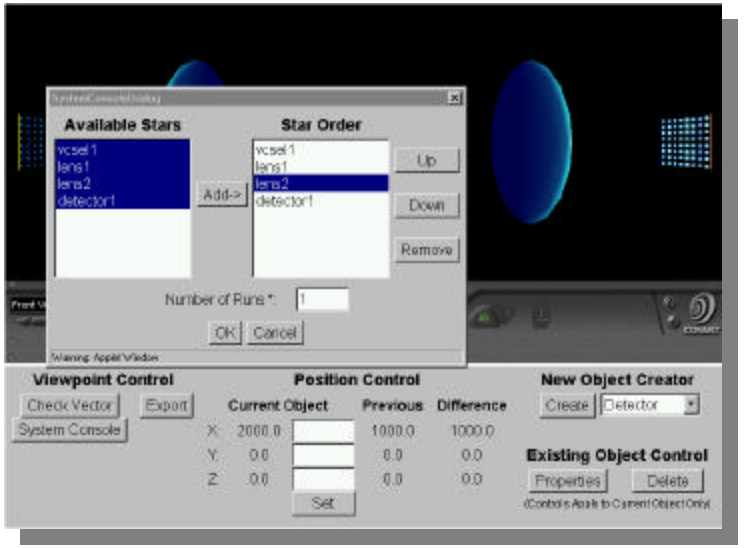


University of Pittsburgh

Return

Chatoyant
3D Graphical User Interface





A new 3D GUI to simplify the creation and visualization of Optical/ Electrical/Mechanical Systems

- O/E/M systems are position dependent
- Intuitive user interface with remote execution
- Replace VEM in Ptolemy

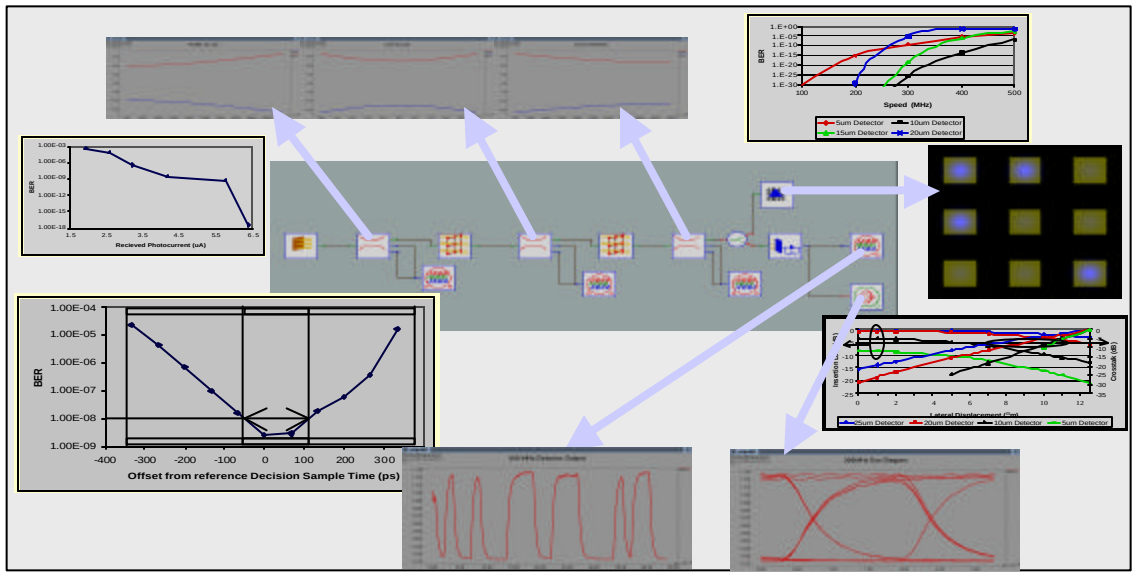
Return

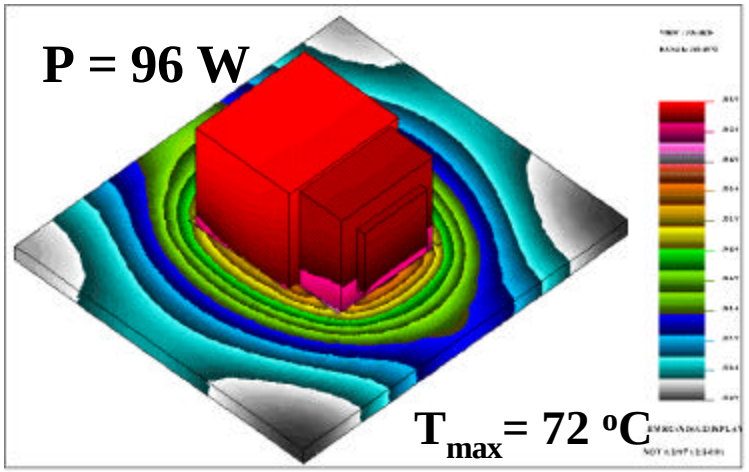
3D OESP Modeling Tools

- Multi-Domain Free-Space OE System Level Simulation and Analysis Tool
- Built on Ptolemy (UC Berkeley)
  - Optical, Electronic, Mechanical models
  - Complex signal types - Geometric, Gaussian, Scalar optical propagation
  - Discrete event simulation with piecewise linear models

CHATOYANT

- Optomechanical analysis tool based on statistical methods (Monte Carlo simulations and design of experiments, regression analysis, prediction models)
- 3D FEM thermal and thermo-mechanical analysis tool
- Rigorous analysis tool for low f/# optics (defocus and polarization effects

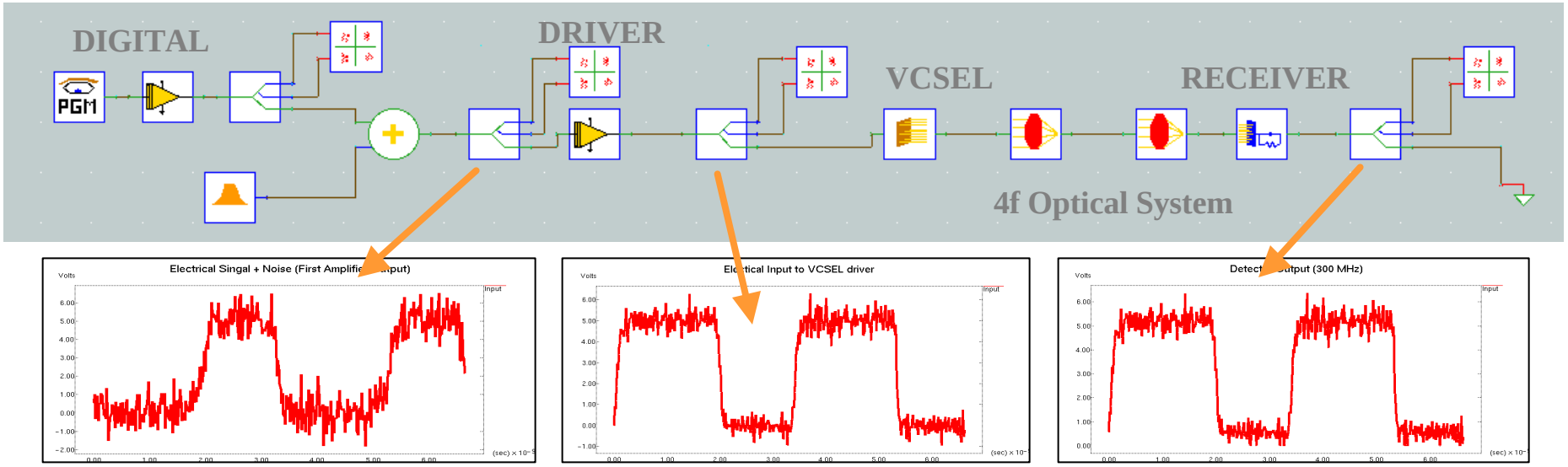




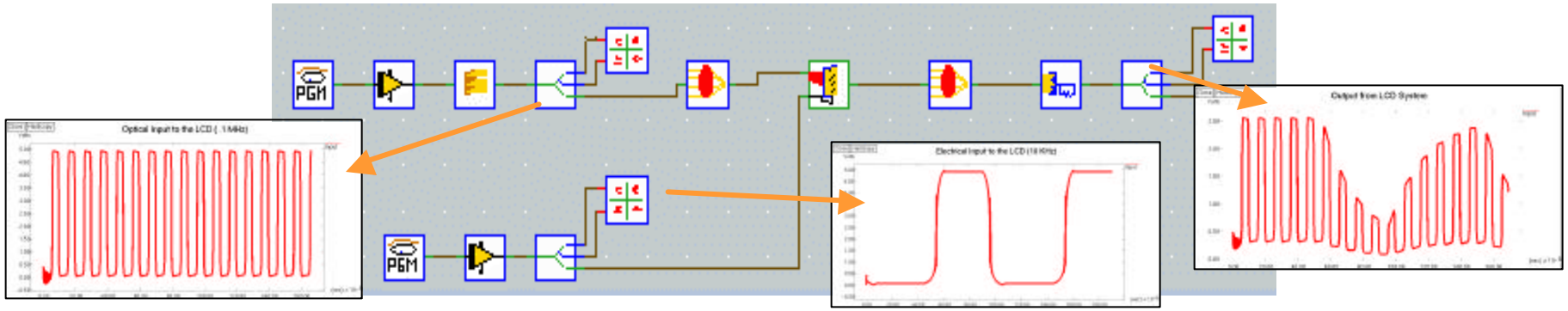
Return

Free-Space Opto-Electronic Modeling and Simulation

Complete *4f* Free Space Optical Link



Multi-rate System: *4f* Free Space Optical Link with a SLM (LCD)



University of Pittsburgh and UCSD

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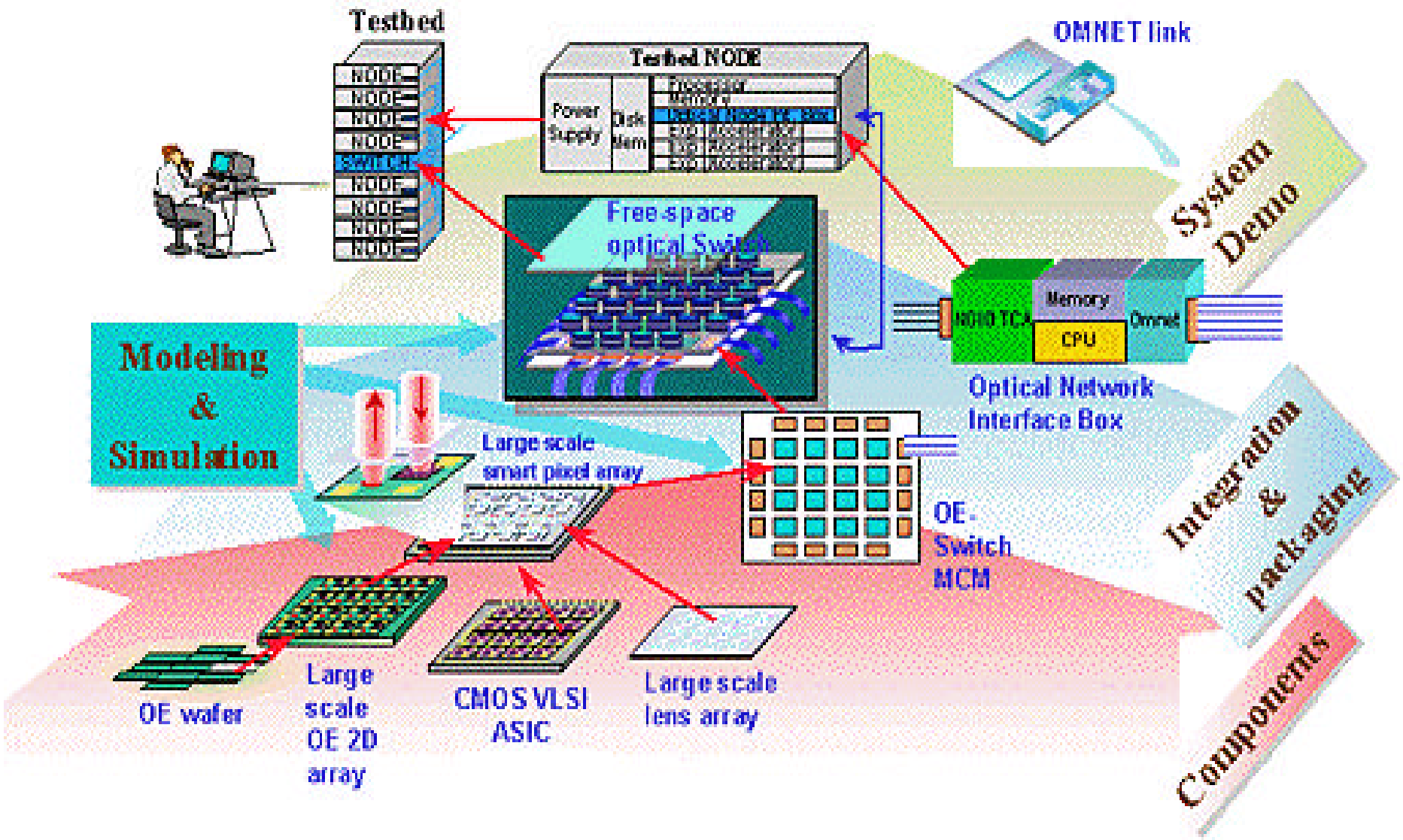
Summary



Return

Summary

Optical Interconnect Challenges and Opportunities

- **Devise technology and architectures to employ:**
  - **Photonics where it makes sense**
  - **Electronics where it makes sense**
  - **Hybrids where they make sense**
- **Compute with electrons, communicate with photons**
- **Optimize energy conversion processes to minimize the effects of entropy on efficiency**
- **Demonstrate credible and clear speed or power advantage over electrical interconnects in multiprocessor communications**

Return

Summary

- **Continued improvements in high-performance computing cannot be sustained by feature-size scaling alone in integrated circuits (Moores Law cannot go on forever)**
- **Develop heterogeneous integration and packaging techniques**
- **Abandon monolithic integration for heterogeneous integration - *"mixed signal component integration"***
- ***However…***
  - ***Current Integrated Opto-Electronic Modeling and Simulation Technology is generally individualized and immature***

Return

Mixed Electronic-Photonic System Design

James Theimer

Return

Mixed Electronic-Photonic System Design

• Build a Top Down simulation

• Benchmark design suite against sets of systems components & devices

• Outcome to be interfaces (I/O) for the modules

• Challenge: Support work to develop a family of modules at different levels of assumed integration
  - OE channel with 40 GB/s data rate
  - Optical interconnects for multi-chip modules
  - 100K element radar phased array with a photonic manifold
  - Synthesis of [VCSELs/EO modulators]/(substitute your favorite component or subsystem)

Return

• Background work supported:
- Models of new photonic devices (bandgap, etc.)
- Innovative (speedy) algorithms - e.g. managing multiple time/length scales, finding ways to uncouple different aspects of a problem

• Anticipated required outputs:
  - Indication when simulation assumptions are being violated
  - Mechanical alignment

• Lower level modules should be designed so they will predict performance under laboratory test
  - Continue to support work in model extraction

- Issues which much be addressed:
    - Packaging
    - Multi-disciplinary group environment
    - 3D layout and visualization

- Established standards protocol for the models and model validation

- “Business model” for transition to commercial product (unless a critical military-only need)

Return

Additional questions

- What is unique about photonics
- what is the big issue in mixed signal photonics
- Is there a basic roadblock to integration of electronics and photonics
- Are there enough users to create a marketplace

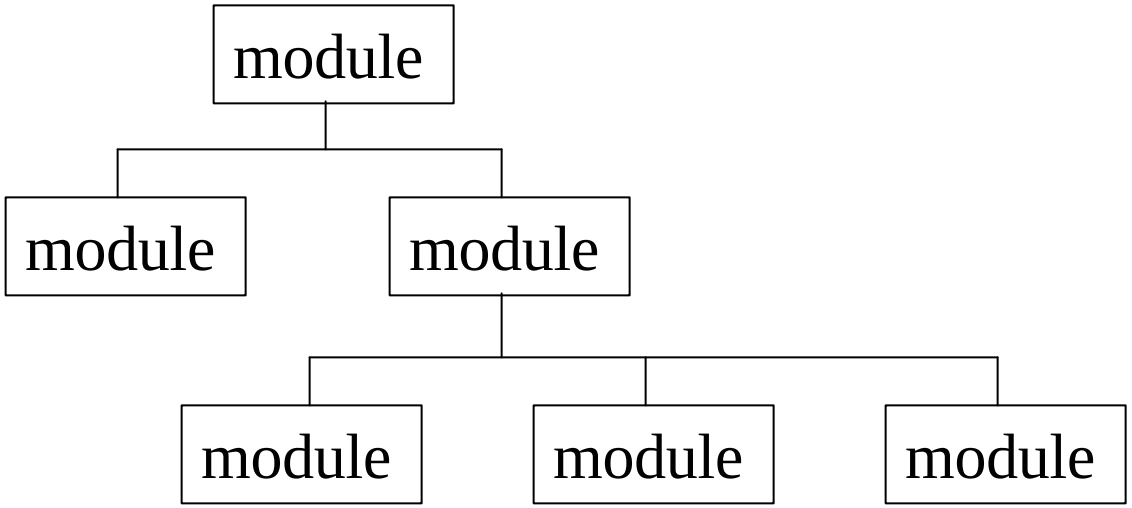
Return

strategy

- How do we control resolution with level of modeling
- What is an appropriate level of abstraction
- What is the most important physics

Return

Top down approach



Return

Top down approach

- Define all the interfaces
- Who will integrate the models
- What existing models are out there
- Zoom to level of abstraction by adding more sophisticated modules
- try to achieve an open framework for adding modules

Return

Module development

- Define a set of “canonical models” that we know will be needed.
- Try to develop automated, nonlinear, context sensitive macro models
  - this is a very hard problem
- Should we go after high fidelity models first

Return

Other comments

- Photonics is different from electronics because it is always operating in a nonlinear regime

Return

My comments (Jim Theimer)

- I described how my effort to do mixed signal design forced me to use excel spreadsheets to track a small number of parameters, such as gain and noise figure
- This approach made it hard to changes technologies, or search the parameter space.

Return

My comments (Jim Theimer)

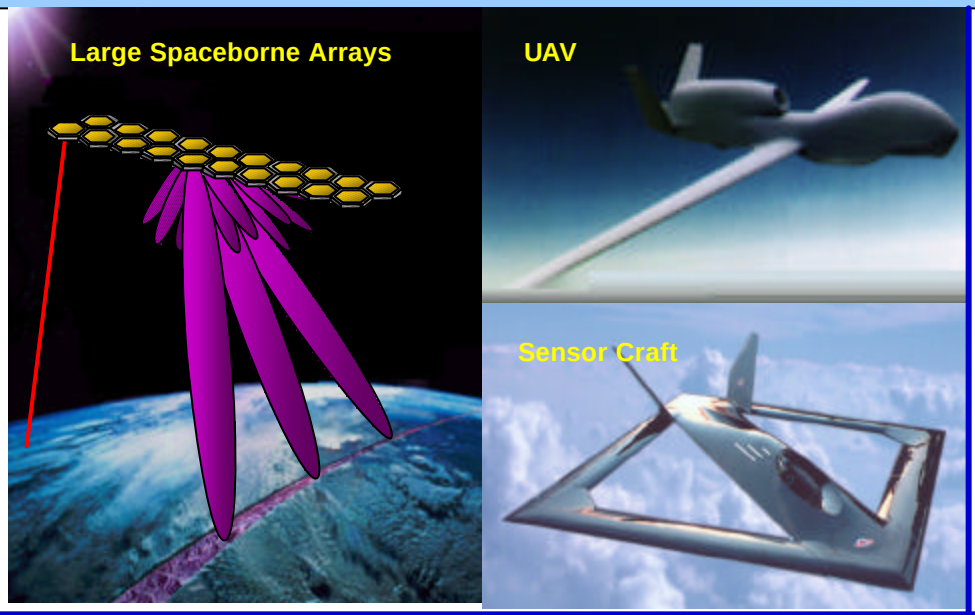
- My experience modeling laser noise showed that I could use hours of computer time just to compute noise statistics. We would like to be able to trade fidelity for speed in some situations
- commercial packages were hard to learn, and could not model phase arrays with hundreds of elements

Next Generation CAD Capability for Future Mixed-Signal DOD Systems

Dr. Greg Creech
Air Force Research Laboratory, Sensors Directorate
October 5, 2000

Return

Digital Beamforming Focus Area



OBJECTIVES:

- Develop & transition digital beamforming (DBF) technology for transmit and receive array antennas to air and space platforms.
- Enable simultaneous multi-beam multi-mission functionality for advanced radar, communications, and EW systems.
- Achieve DBF insertion within windows of cost, manufacturability and maintainability

APPROACH:

- Leverage outputs from enabling technology programs: A/D, D/A converters, DDS, FPGA and ASIC parallel processor architectures
- Develop wide scan, wideband, multi-beam architectures and beamforming algorithms for conformal and planar array apertures
- Address platform self-interference effects

Return

Modular Digital Radio Frequency System **(MODRFS)** Program

Objective: To prove through demonstration that future state-of-the-art avionics can be developed using a “building block” systems architecture.

RF Building Block (BB) Approach:

- Examined Radar and Electronic Warfare Requirements.
- Identified Functional Subsystems (Aperture, RF Electronics, Processing)
- Further identified isolation layers at physical/functional boundaries (Common Interface)
- Defined RF BB Specifications

Benefits:

- Maintain highest performance throughout System life-cycle
  - Plug & Play RF BB
  - Gracefully incorporate technological advances
- Supports higher levels of integration thus increased reliability
- Reduced Cost through REUSE
  - Common Module interface across functional subsystem
  - Common RF BB across module type

Return

MODRFS Will Impact A Large Number of System Insertions

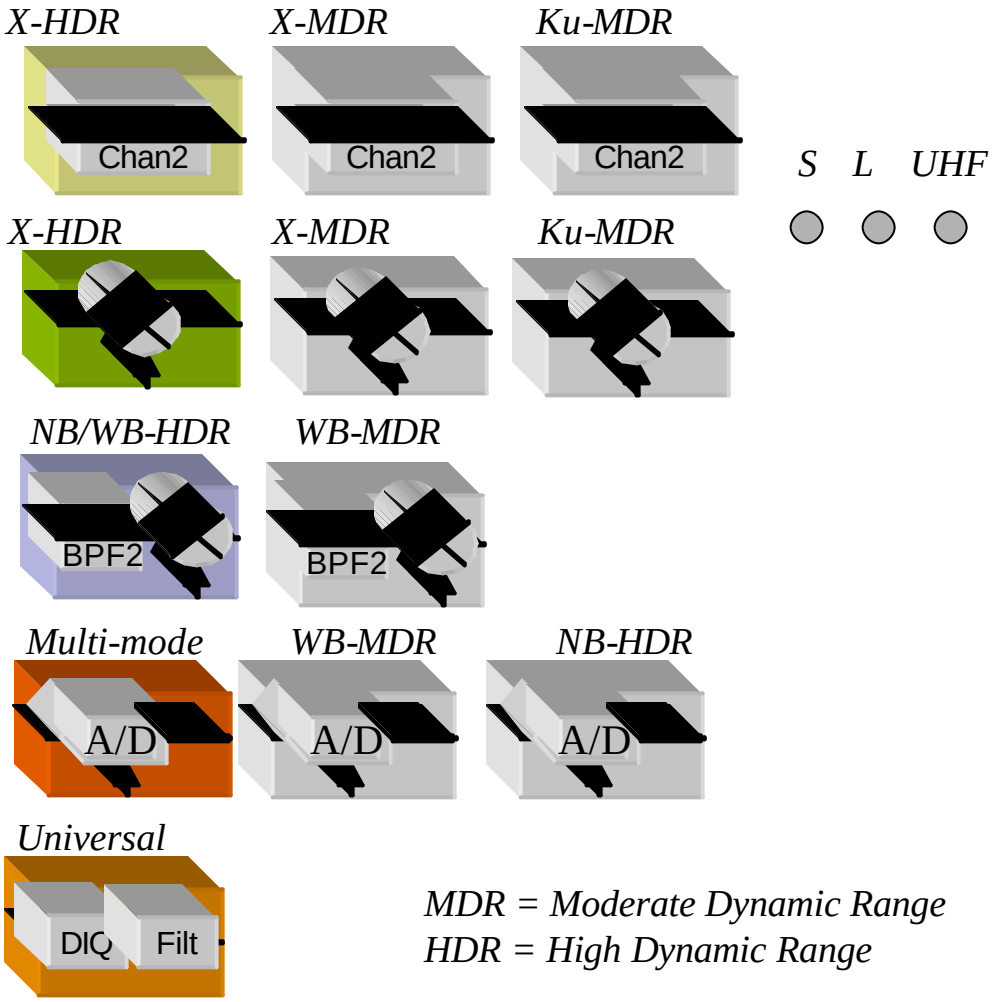
BB1-*RF Filters*

BB2-*Downconverter 1*

BB3-*Downconverter 2*

BB4-*A/D Converter*

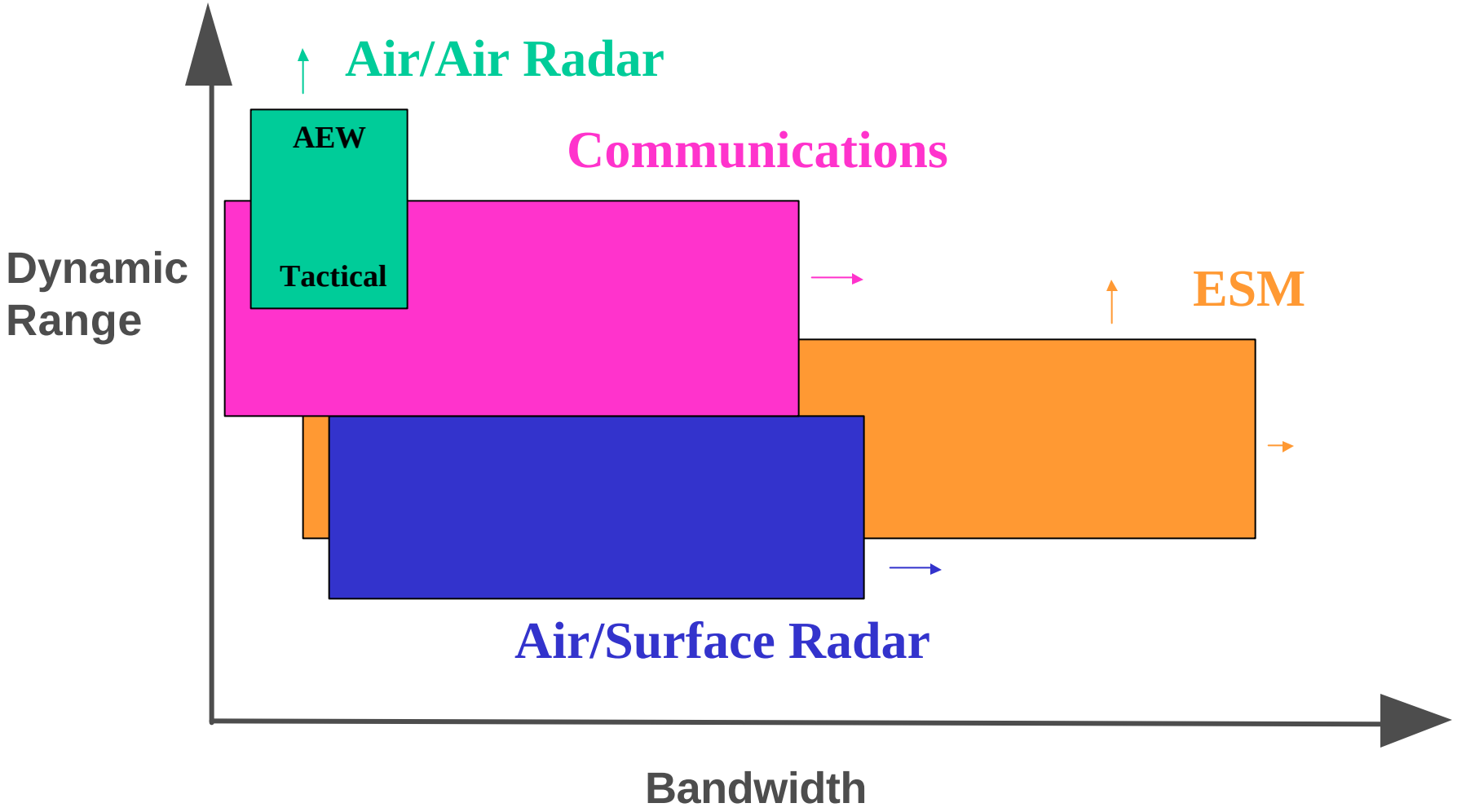
BB5-*Digital Preprocessor*



MDR = Moderate Dynamic Range
HDR = High Dynamic Range

Return

Typical Receiver & Exciter Requirements Across Functions



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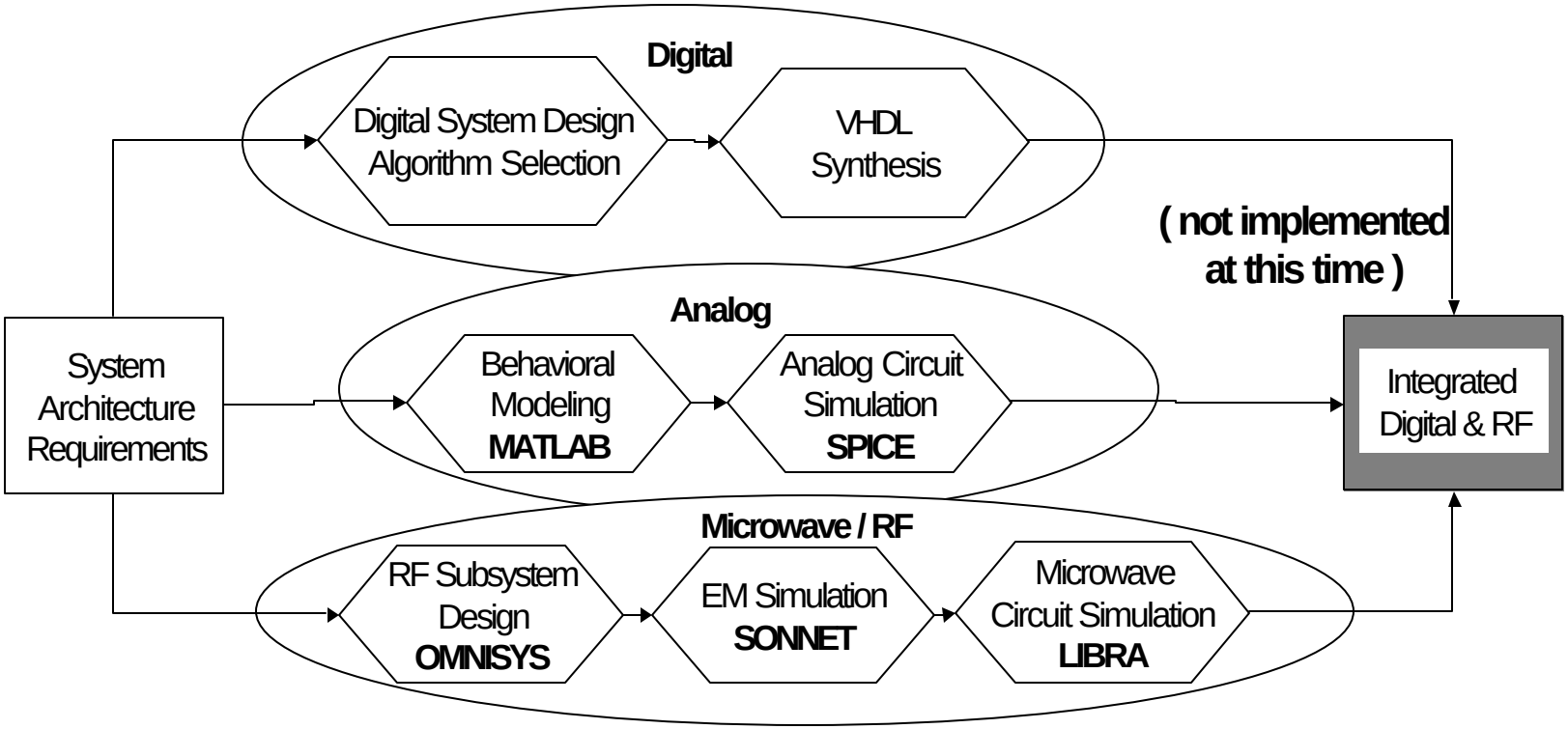
Current Simulation Approach



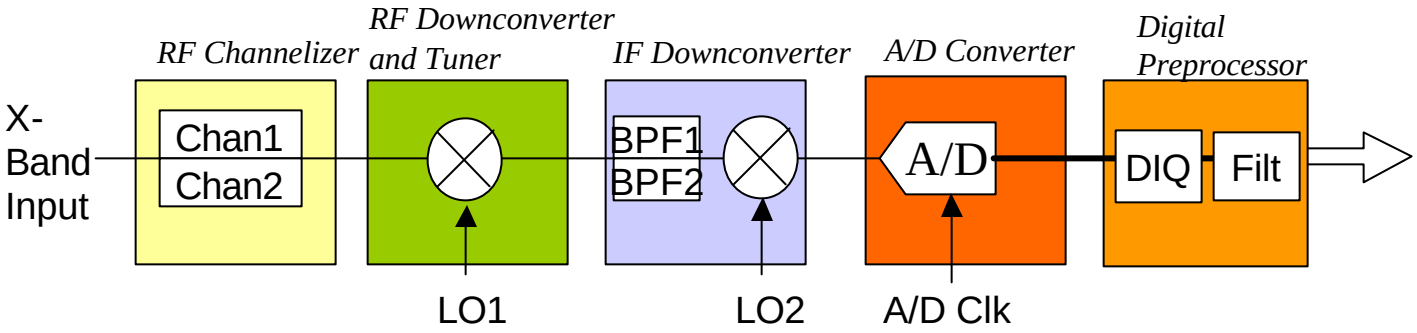
Simulation Approach Varies By Circuit Type (Simulation Domain)

Return

Simulation Domain

- Mixed-Signal Simulation

Receiver Partitioning

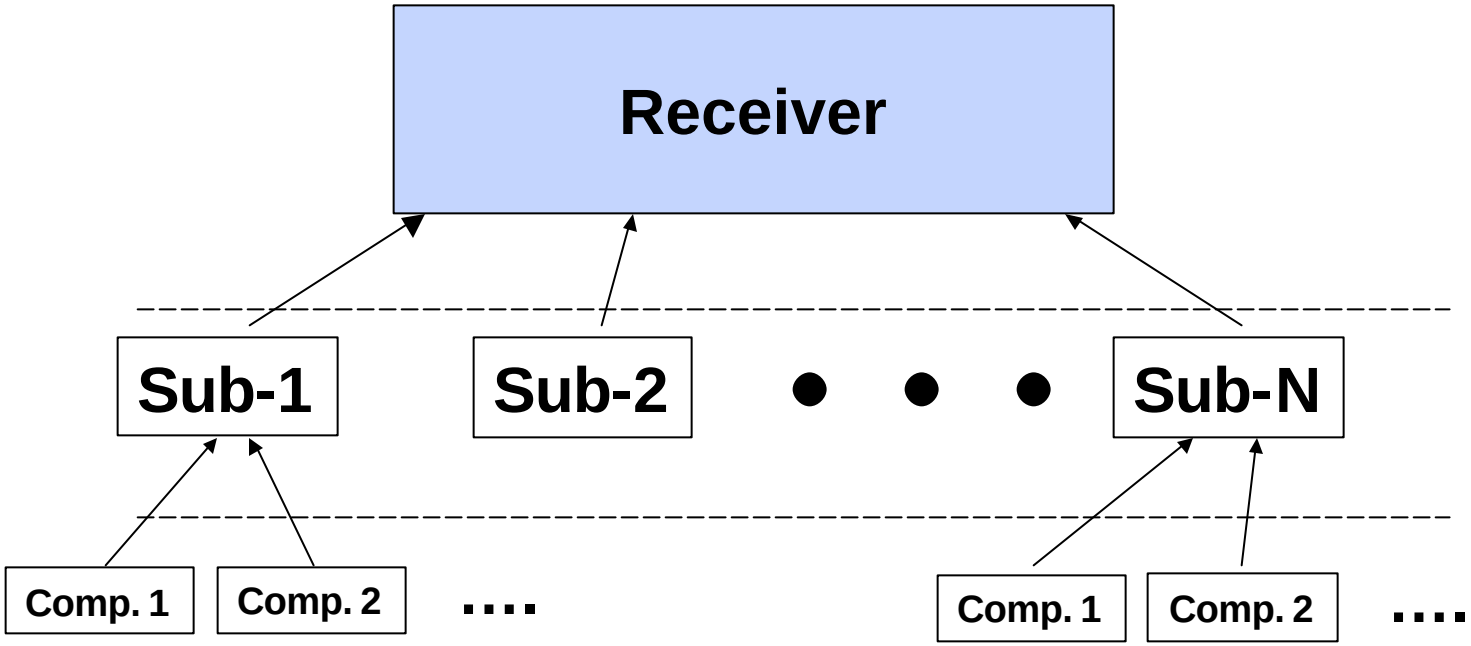


Frequency----------Time----------Digital

Define Signal Interfaces

Return

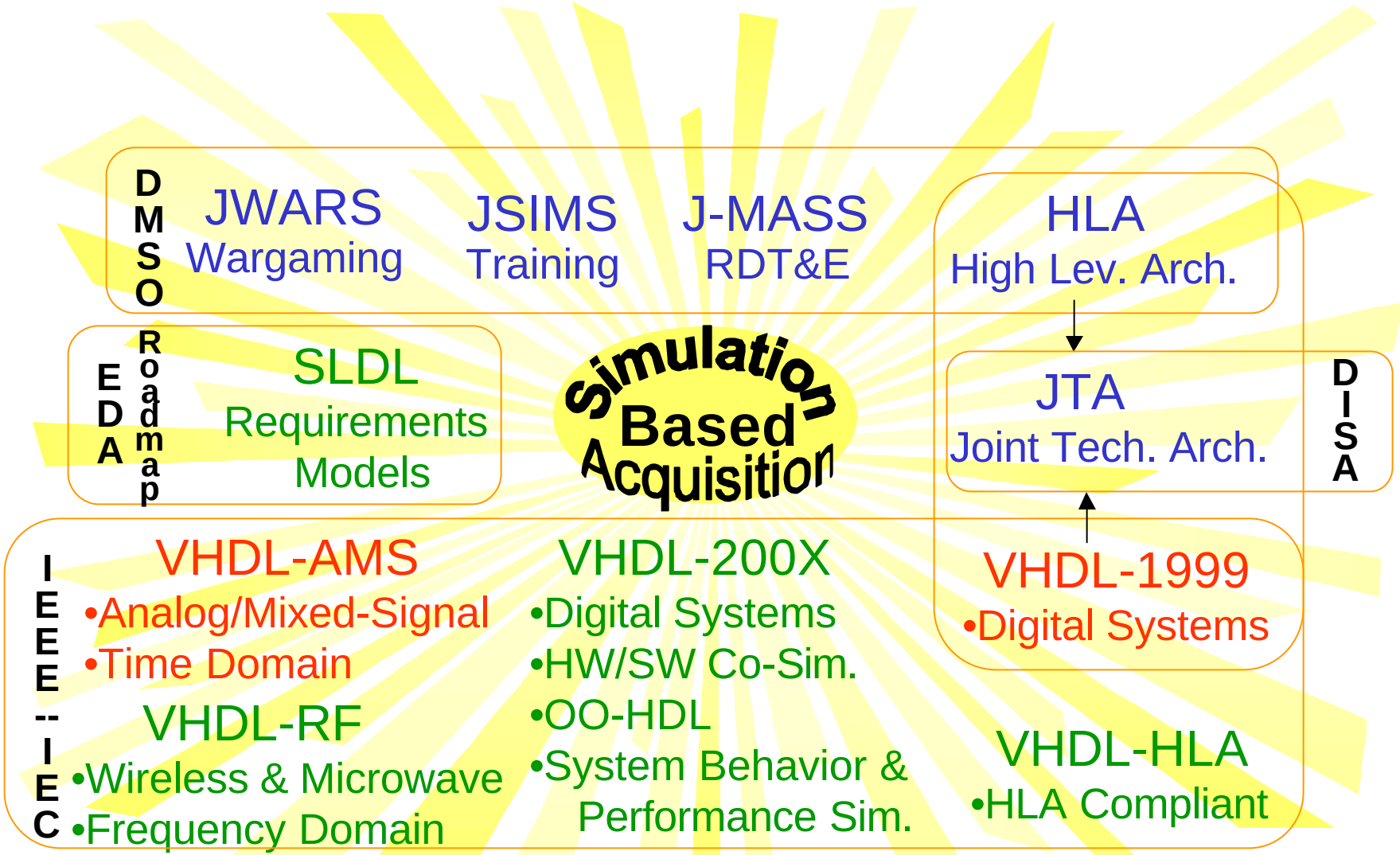
Specification Partitioning



Define Design Hierarchical Interfaces

Return

Modeling & Simulation Standards For Simulation Based Acquisition

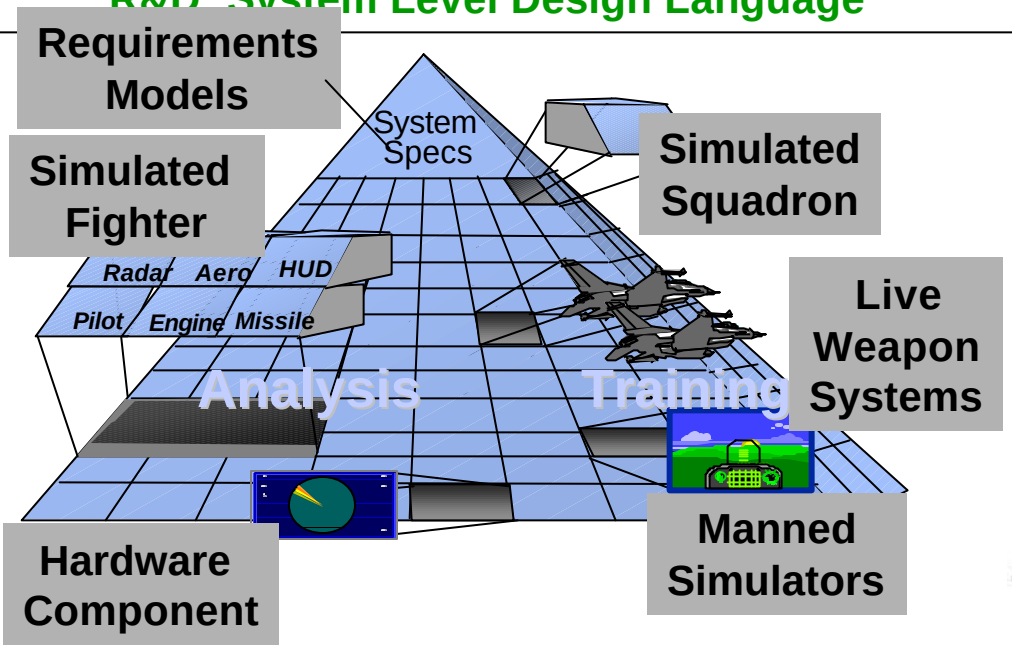


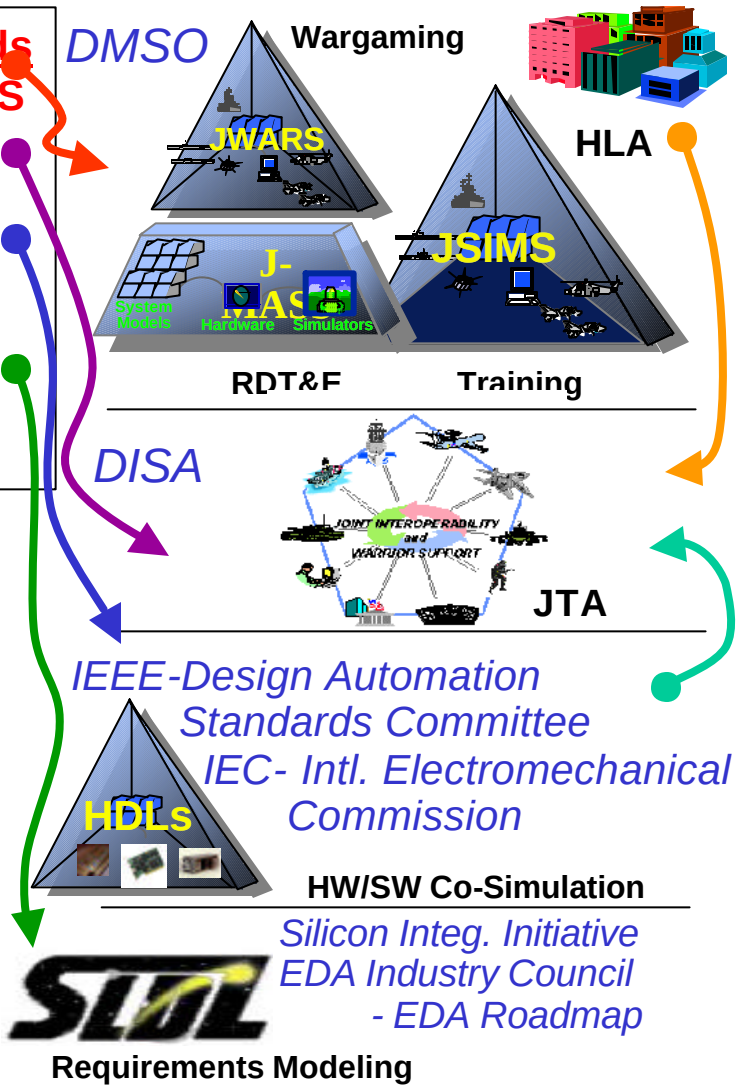
DoD Std. AF R&D A DoD Influenced Industry Std.

Return

DoD S&T Is Driving Toward An Integrated Set Of DoD & Industry M&S Standards For Joint Warfare Simulation and Simulation Based Acquisition

Defense Modeling & Simulation Office Joint Standards
DoD High Level Architecture, J-MASS, JWARS, JSIMS
Defense Information Systems Agency
Joint Technical Architecture
Hardware Description Languages
Industry Stds.: VHDL, VHDL-Analog Mixed Signal
R&D: VHDL-200X, VHDL-RF, VHDL-HLA
Requirements Modeling Language
R&D: System Level Design Language





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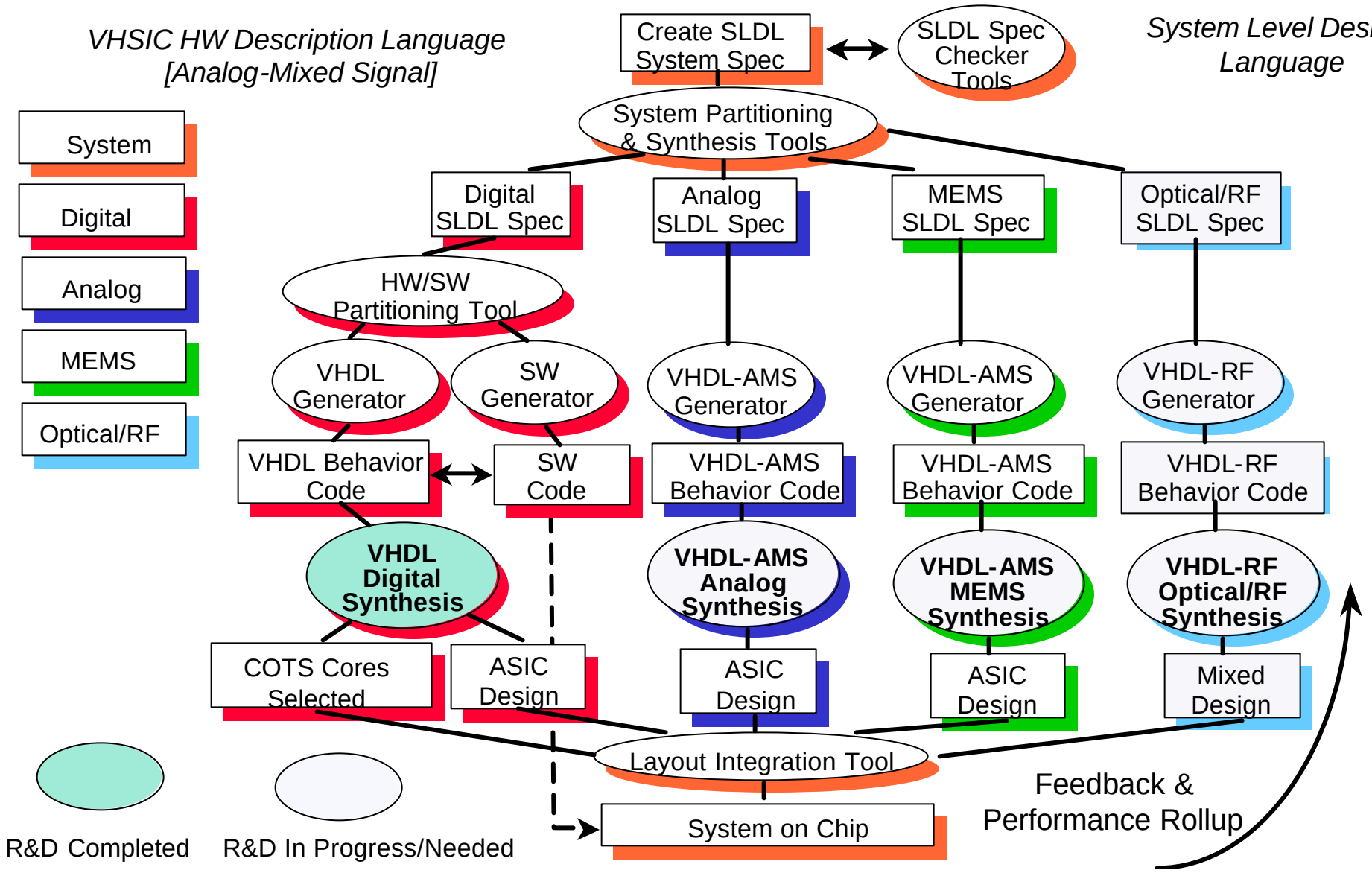
Vision For The Integrated Design of Systems on Chip



Return

Systems on Chip Design - Things To Do

VHDL-AMS Language Enhancements -> VHDL-MS

- Add partial differential equations for Optical, Fluidic, EM
- Add frequency domain and distributed parameter features
- Develop Noise Models for device and circuit models.
  [temp., supply voltage, current, photonic, radiation, substrate, & ??]
- Develop VHDL-AMS frequency domain simulator/solvers

Mixed-Signal Synthesis

- Parasitic driven Mixed-signal synthesis & Optimization
- Develop Topology Selection Tool and Library of Topologies
- Develop parameter selector and smart Mixed-Signal auto-layout tools
- Develop Fab-based analyzers for reliability, manufacturability, yield
- Automated test generation for mixed-signal systems

System Level Design

- Formal specification of mixed-signal system rqmts. (SLDL-Rosetta)
- Partitioning and Synthesis from SLDL- Rosetta specifications
- Mixed discrete event (digital), continuous time domain (A/D, D/A),
  and frequency domain (RF/Optical) simulation
- Verification of properties like power, noise, bandwidth, higher frequency behavior

Web-Based Collaborative Engineering

Return

Analog and RF Functions Dominate the Cost of DoD Systems; Reduce Their Cost By Automating Analog and Mixed Signal SOC Design

- Analog/RF Design Is About 70% of Cost Of Electronic System Development
- Analog/RF Design Is Manual Except For Simulation
- Analog/RF Design Is Very Difficult Compared To Digital Design
- Analog/RF Designers are Rare and In Demand By Consumer Electronics Industry
- Analog/RF Circuit Designs Take Much Longer Than Digital Designs
- Analog/RF Designs Don't Scale With Transistor Size (i.e. can't reuse)

Analog/RF Circuit Applications

Signal Filters
GPS Receivers
Signal Comparators
Serial Port Interfaces
Frequency Synthesizers
Analog to Digital Converters
Digital to Analog Converters

ID Friend/Foe Transponders
Backplane Bus Transceivers
Amplifiers and Pre-amplifiers
Modem CODECs (coder/decoders)
Wireless Transmitters and Receivers
Liquid Crystal Display Dot Matrix Drivers

Smart Batteries
Power Supplies
Speech Synthesis
DC-DC Converters
Voltage Regulators
Automatic Gain Controls
Modulators/Demodulators

LASER and LED Drivers for Fiber Optic Systems
ISDN, ATM and other Network Interface Transceivers

Wired & Wireless Audio, Video, and Data Transmission
Signal Compactors/Expanders/Spreaders/De-spreaders

Opto-Sensors (Light-to-Frequency and Light-to-Voltage) for Fiber Optic Systems
Motor Servo Drivers and Control of other Mechanical Systems (e.g. pointing antennas)
Interfaces to Sensors (CCD's, Radar, Infrared, Corrosion,Temperature, Pressure, Motion, Laser, Strain, Chemical, Nuclear, Biological, etc.)

Return

TECHNICAL BARRIERS

- **Faster Simulator/Solvers**
  - **[Parallel Processing, Distributed Processing, Reconfiguable Computers, Hybrid Analog & Digital …]**
- **Accurate non-linear Reduced-order modeling (Macro-models)**
  - **breakthrough innovation required**
- **Simulators for VHDL-AMS are much more difficult to develop than for VHDL digital only circuits**
- **Full Spectrum Optical/RF/Analog/Digital Integrated HDL will be tricky because of multiple domains**
- **Mixed-Signal circuit synthesis is hard because of layout effects**
  - Conducted, Coupled, Radiated, Thermal energy
- **Integrating all of the pieces for Web-based collaborative engineering**
- **Building industry consensus for standardization**

Return

Concurrent Mixed Signal Design

Problem/Need:

Products containing digital, analog, & RF components are currently designed using different design environments & Tools & thus do not allow interactive simulation of the entire design as a whole to simulate performance. RF & Digital/DC Interaction & coupling is not accurately incorporated.

Functional Needs:

- **Rapid Large Complex Design Simulation** - Ability to Simulate complete Large designs using complex Modulated signals at once in a reasonable run time. Future designs will continue to grow in size/complexity.
- **Incorporate Digital /RF Coupling Effects** - Ability to simulate pwr supply Line feed through,clock noise, line coupling effects, & handle distributed transmission lines caused by the physical layout/Line routing .
- **Automated Layout & Design Synthesis** - Automated or assisted routing for layout generation of complex designs which take into account line shapes & parasitic coupling associated with RF on the same component.
- **Co-Time/Frequency Domain Simulation** - Selection of optimum simulation domain.

Return

Concurrent Multi-View Design

Problem/Need:

Mechanical & electrical views of a design are currently captured independently, requiring design iterations. Impacts/interdependencies on electrical, mechanical, thermal, cost & durability are needed as each design view is captured.

Functional Needs:

•**Portable Single Data Model Representation** - All attributes of an object needs to be captured once and be useable across the different simulation views with not manual re-entry. Ability to integrate design specifications, geometry/features, material characteristics, and manufacturing rules/methods along with user defined analysis algorithms is needed.

•**Real Time Optimization Impact Assessment Across Multi-views**- Optimization in the electrical view will automatically update the mechanical view & determine impacts in the mechanical or thermal or cost. Design Environment warning of violations in one view caused by changes in another view.

•**Inter View model Transform Mapping** - Inter Domain Model Transform Mapping is the ability to determine the effect of a change in one domain in the other domain. An example would be the electrical characteristic of a MEMS switch due to a change in the mechanical structure. A similar case is the goal to do electrical simulation from layout. Future needs will require expansion to electrical to cost domain, thermal,durability. Another example would be being able to map the model of Pout for an HPA to the Cost domain.

•**Single GUI for symbolic Design Representation** - A common Graphical user interface to an object that will be the same for use in mechanical, or electrical, etc. views.

Return

Hierarchical Multi-Level Design

Problem/Need:

Specification Partitioning/Requirements flow down from system to component has been done without adequate consideration of component capability. The Design system is needed to aide in this process to achieve an optimum design.

Functional Needs:

- **Portable (between levels)simulatable behavioral models** - Behavioral models need developed with the inclusion of the right influencing factors that are usable in simulation tools at the MMIC, MCA/MCM, subsystem levels.
- **Flow-Down of Executable Specifications to lower levels** - Higher level system Specifications need to be simulatable at lower levels. Simulation parameters at lower levels are not always easily related to higher level parameters of interest. (Gm doesn't mean much to Subsystem designer)
- **Capability Flow-up** - Impacts on Requirements flow-down must be rapidly determined & advised by the design System during initial spec partitioning/preliminary design .
- **Selectable Levels of Behavioral model Abstraction** - Multiple levels of abstraction in terms of complexity & capability are needed along with rapid generation tools/capabilities.

Return

Selectable Fidelity Behavioral Models

Functional Needs:

- Generic & specialized library components
- Hierarchical model translator
- Existing model translators
- Enhanced simulator/simulator control(abstraction)
- Integrated schematic editor(symbolic, textual)
- Template based model generator
- Backannotation tool (Hierarchical levels)
- Optimizers

Status/Technical Issues:

- Behavioral models are in use for digital design & are expanding to Analog design. Initial attempts are under way for RF design.
- NO common HDL exists/is in use to allow model portability
- Existing models do not include all required influencing parameters/effects, thus are not accurate enough.
- Choosing the desired level of fidelity for passing up models vertically in the hierarchy is limited.

Return

Product Development/Data Management

Problem/Need:

To optimize a Complex design across Mixed Signal, Multi-view,Multiple Hierarchical levels, multiple organizations & tools, an overall Product/ Data management system is needed. An Enterprise Design system is key.

Functional Needs:

•**Design Advisors & Risk Advisors** -Guidance to Ensures an established design procedure/discipline is used in capturing the optimum design.

•**Configuration/Version Control** -Tracking of all versions & models used in the design capture phase.

•**Requirements/Specification Tracking** - Documented tracking of requirements, specification partitioning status,& specification priority

•**Schedule(Status)/Cost Tracking** - On-line browsing of schedule and cost tracking/prediction during development & production.

•**Design Database Control** - Ensures database management & interface to design system.

•**Design Verification** - A product verification guided procedure/tracking via test, inspection, simulation or analysis of measured data is required.

Return

Enhanced Component (MMIC) & MCM/MCA Assembly Design Library Kits

Problem/Need:

The Design Library Kit is the data/information required to completely describe/represent the foundry capability. It contains models, DRC, ERC & info for cost/yield predictions.

Functional Needs:

- **Common formats** - Common formats useable by multiple EDA tools to allow user selection/comparisons of foundries for a given design.
- **Library Expansion for Design to Cost & Durability** - Information for cost/yield predictions/design.
- **Rapid library/model generation capability** - Rapid library/model generation capability is needed for new technology/process/device changes.
- **Electronic Vendor Parts Descriptions** - More compatible Vendor parts descriptions for design capture.

Return

Interoperability Standards/Approaches

Problem/Need:

Standard Interfaces is the key to many concurrent design tasks which involve data transfer & multiple tool use.

Functional Needs:

- **EDA Vendor Tool to Tool Design Transportability Stds** - Standard "socket" for access to multiple supplier's simulators within any environment. This would provide designers with a choice of simulator best suited for a particular application.
- **Foundry Library Kit Format Stds** - Foundry Library & Vendor Component formats are needed & must be adopted for Designer foundry/component selection/comparison.
- **Hierarchical Level to Level Design data Portability Stds** - Portability of behavioral models/ data to different levels that are simulatable requires a std interface.
- **Inter-View Design Data Portability**(Electrical-Mechanical, etc.) - Inter-View portability will require 3D geometry Stds.
- **Design to Manufacturing Interface** - An electronic link between design environment & automated manufacturing/assembly machines.
- **Design to Test Interface** - Capture & Transfer of test information during the design process & create an automated test plan.

Return

CAD for Analog, Mixed-Signal, & RF

Moderator:

Rob Rutenbar

CMU

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Process

- Brainstorming critical issues
  - What matters? Why? Where?
- Understanding DOD unique requirements
  - Ex: $$$ less critical than performance, not TTM-centric, but time-to-tech-freeze matters
- Result: 17 topics discussed
  - Weighted voting: 8 votes per person, arbitrarily allocatable over the topics
  - Separate tallies: “DOD” folks vs “commercial”

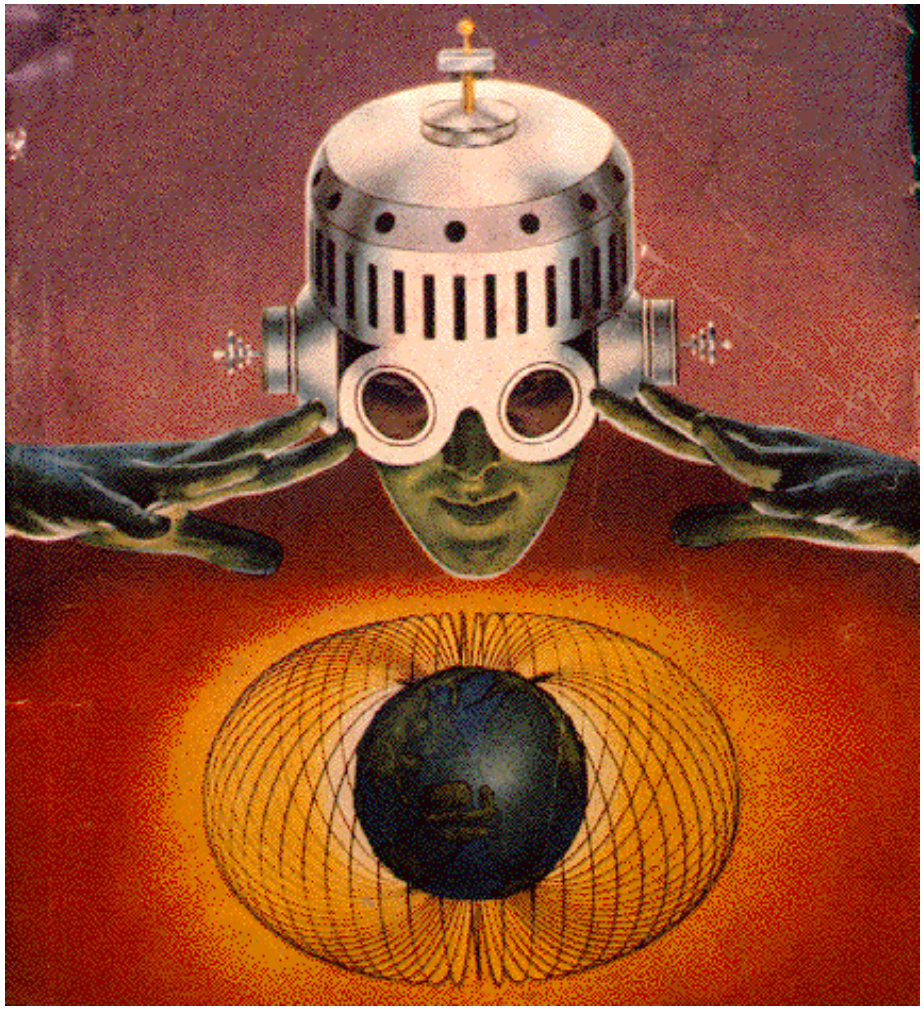
Return

DOD Requirements…

Very different than typical commercial specs

Example, when using your cell phone, nobody is trying to “home in” on it, jam it, shoot you

(Example next-gen DOD-system, artists concept…)



Return

DOD Requirements

Performance matters most

Cost is less important…

Return

Critical Topics, Areas, Issues

1. Nondigital designs in "esoteric" tech (need for real models), low-level & high-
2. 2D? 2.5D? 3D? 1chip? 2? (NB --$$ not critical)
3. Fast(er), full EM sim, massive coupling
4. Other num solvers && analysis && checker tools (eg, Long-time transient sim)
5. Plumbing (integration), standards, common APIs, interop? (intell prop issues)
6. Auto modeling, nonlin model order reduction (physics->ckts->behavr) && charactrz && empirical modeling
7. Specs, hierarchy, cross-domains, verification, tstbnch
8. Increasing # student designers, CAD devel; MOSIS issues; expertise capture (wizards)
9. Reconfigurable, soft platforms (emulation)
10. Synthesis! / IP / reuse
11. Migration, design longevity
12. Noise / immunity / isolat
13. Statistical design/optimiz
14. Nondigital design, robustness in aggressively scaled CMOS
15. Multiple domain simulation, modeling, abstract, codesign (mixed-signal too)
16. Test && fault modeling && formal verification
17. Visualization / navigation

Return

Weighted Results: DOD Folks

22 Synthesis/IP reuse
20 Fast full EM simul
12 Auto nonlinear modeling (physics -> behav)
9 Design in esoteric processes
8 Better general num solvers
6 Noise
6 Mixed domain simulation
5 High level spec languages
4 Reconfigurable platforms (analog fpga)
3 Robust ckts in deeply scaled CMOS
3 3D chip integration
2 Test
2 Tool plumbing & integration
1 Long longevity design migration
1 Educate more analog designers

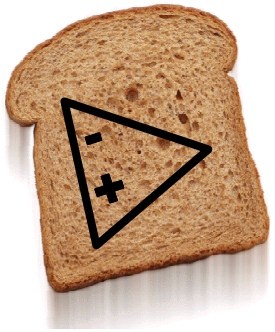
Weighted Results: non-DOD Folks

33 Synthesis/IP reuse
31 Auto nonlinear modeling (physics -> behav)
24 Fast full EM simul
12 Mixed domain simulation
8 Better general num solvers
7 High level spec languages
7 Noise
7 Design in esoteric processes
7 Test
5 Tool plumbing & integration
4 Reconfigurable platforms (analog fpga)
3 Statistical design
3 Long longevity design migration
3 Educate more analog students
2 3D integration
2 Robust ckts in deeply scaled cmos
1 Better visualization / navigation of large data sets

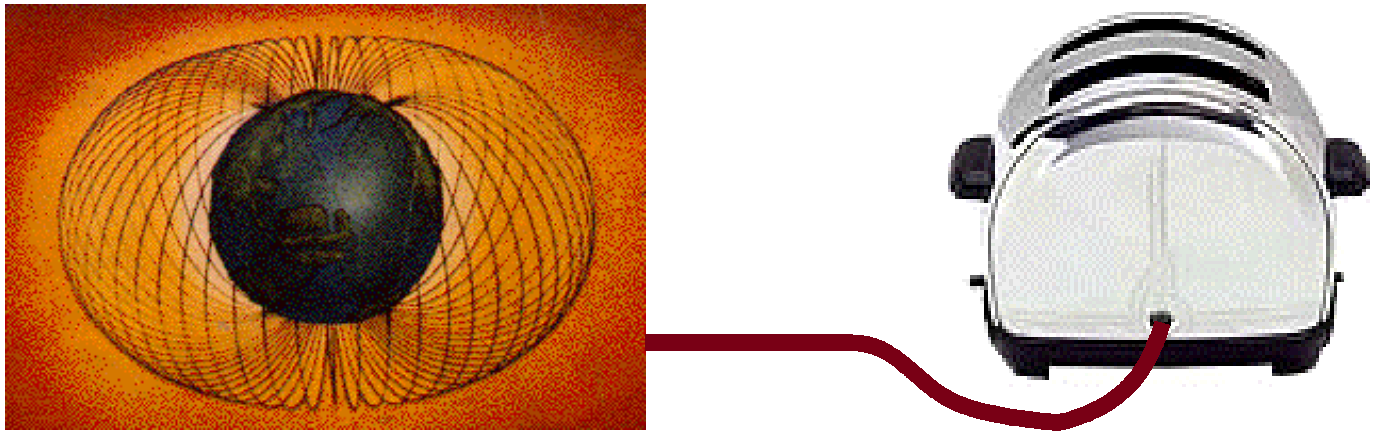
Return

Surprising Support For…

Synthesis, auto modeling, good models in ALL forms, for ALL processes



Unsurprising support for "serious" simulation in ALL forms…



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Surprising Lack of Support for

Flows and similar plumbing

Educating new analog designers

Return

Design of Mixed Signal Systems

Joe Jensen

Oct. 5, 2000

HRL Laboratories

3011 Malibu Ca. 90265

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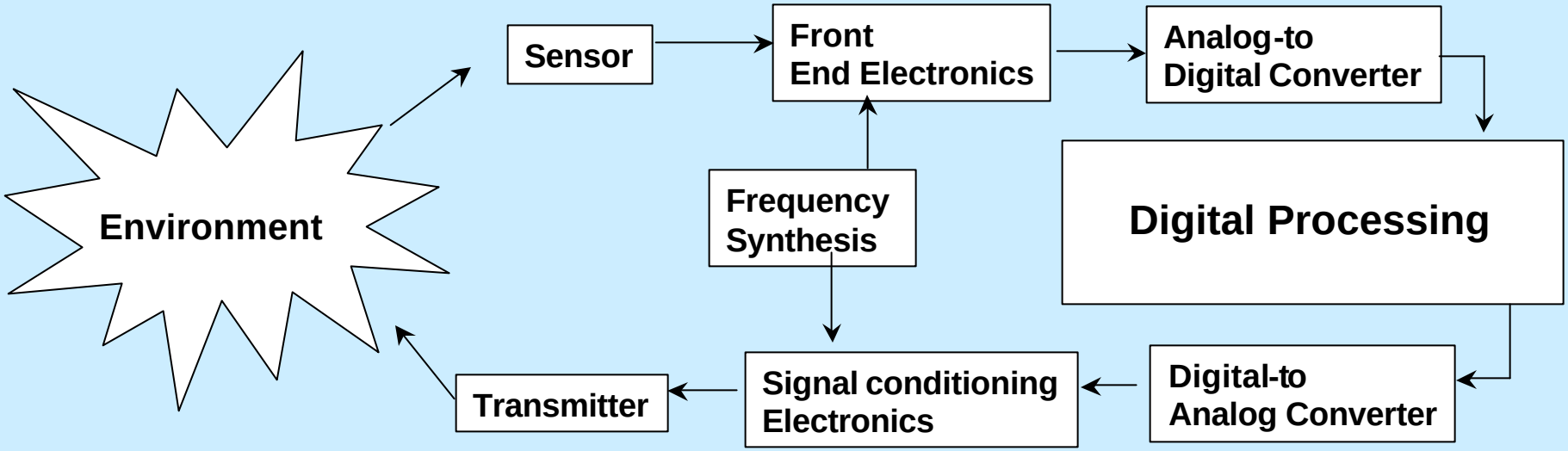
Introduction

- Military systems are rich with mixed signal environments and have higher percentages of analog components than commercial systems
- Mixed Signal ICs in military systems need higher dynamic range over a wider bandwidth than commercial systems
  - Designs are at the cutting edge of technology with little design margin
  - Digital circuits at the analog interface operate at very high clock rates where current digital design techniques break down
- Mixed Signal system complexity is increasing
  - Design and prototyping costs are increasing at a faster rate due to the trial and error approach of mixed signal system design

Return

Mixed Signal Systems Provide a Digital Interface to the Analog World



- Classes of mixed signal circuits include:
  - Front end and signal conditioning electronics
  - Data conversion electronics
  - Frequency synthesis electronics
- Current trends:
  - Move the digital interface closer to sensor or transmitter
  - Embed more analog function into the Digital Processing

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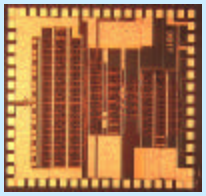
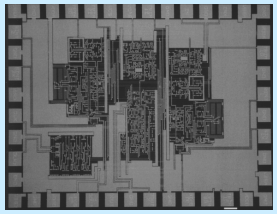
InP HBT Mixed Signal IC Examples

AFWL Funded Program

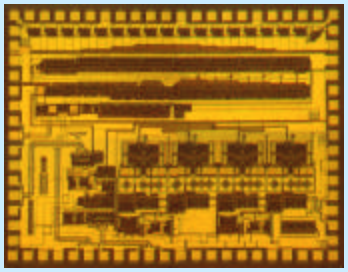


8 Gsps, 3 bit ADC

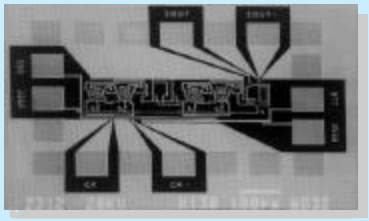
DARPA Funded ADC Pilot Line Enhanced ASIC Yield



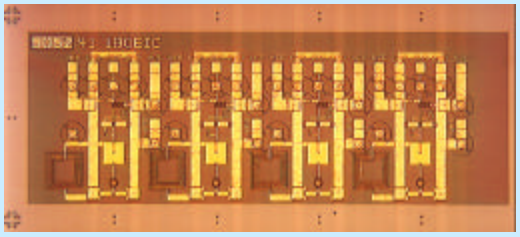
Low Pass DS ADC



4th order bandpass DS modulator with 1:16 DEMUX

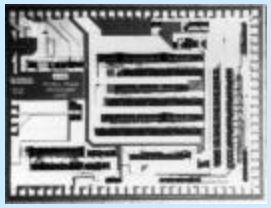


STATIC DIVIDER, MUXES, DEMUXES,

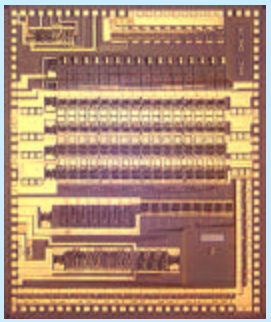


4-CHANNEL OEIC RECEIVER ARRA

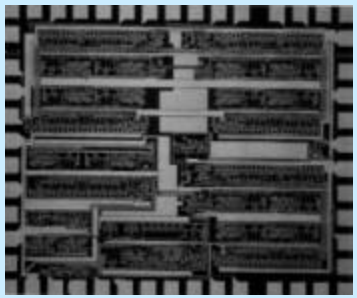
WIDEBAND (1.2 GHz - 18 GHz)



Govnm't Funded Integrated Optical Receivers



12-BIT DAC
-60 dB SPUR-FREE
@ 1 GHz



Phase Lock Loop IC
14 GHz Divide by N counter
4 GHz Reference couter
Phase Detector

Return

The Mixed Signal Design Problem

- The analog components in mixed signal systems do not enjoy the same rate of improvement as digital circuits as technology improves
  - Analog design problems are much more difficult for a given circuit complexity
  - Analog and mixed signal design tools do not provide a comprehensive tool solution
  - Design approaches rely on a designers intuition with a high degree of trial and error

Return

Why are Mixed Signal ICs Difficult to design ?

- Mixed Signal ICs design crosses over many engineering disciplines
  - Digital signal processing
  - Digital design
  - Analog techniques
  - Transistor level circuit design
  - Transistor modeling
  - Noise modeling
  - Microwave and electromagnetic design understanding
  - Knowledge of high speed test techniques

Return

Digital Design process

- Design top down
- VHDL or C software model used to simulate top level behavior
- Synthesis tools used to generate gate level description
- Synthesis tools used for generation of chip layout using existing cell libraries
- Backannotation tools extract simple 1st order layout parasitics (delay calculation only)
- Timing simulation performed with simple first order behavior models of logic gates
- Transistor SPICE simulations only used for development of cell library and logic gate timing models

Return

Analog Design process

- Step 1: Design should begin top down
  - Behavioral models should be used to model top level behavior
  - Analog High Level Description Language (AHDL) not well developed or widely used
  - Tools include: C programming, MatLab, Mathcad, etc.
  - Limitations:
    - Mathematical models do not easily account for second and third order effects.
    - Parasitic and other circuit level effects are not tractable to model in a MatLab or C-code environment
- Step 2: Synthesize analog block level description
  - Analog synthesis tools generally do not exist
    - Cutting edge analog designs are generally full custom
  - Synthesis of the analog block level diagram is generally a manual process

Return

Analog Design process (cont.)

- Step 3: Develop behavioral circuit simulation (SPICE like) simulation model using high level components
  - Capability is somewhat available in commercial CAD but interface could be dramatically improved
    - Interface to high level analog components and digital components should be provided at part of the analog simulator and not an add-on requiring new licenses to be purchased
    - Simulator should be capable of mixed mode microwave/analog/digital simulation
    - Should be provided at a reasonable price to user
- Step 4: Design optimize analog and high performance digital building block cells
  - Analog cell libraries generally do not exist for the highest performance mixed signal ICs
  - Analog designs are re-optimized for each new application
  - Standard SPICE or Libra simulations are adequate

Return

Analog Design process (cont.)

- Step 5: Substitute transistor level analog and digital cells into circuit level behavioral model
  - Functions substituted incrementally and re-simulated as you build complexity
  - Simulation times increase dramatically as more complexity is simulated
- Step 6: Full transistor level simulations are necessary to model complete circuit behavior
  - Transient analysis is usually required for most mixed signal simulation
    - Simulation run times can be as long as several weeks

Return

Analog Design process (cont.)

- Step 7: IC Layout
  - Layout is still full custom for highest performances ICs
  - Layout of cell libraries
  - Place and route of IC interconnect
    - Signal integrity and parasitic at critical at this step
    - standard router do not cut it
- Step 8: Backannotation of parasitics for re-simulation
  - 1st order extraction of layout parasitics are not adequate to model analog behavior.
  - More complex extraction techniques are need to model transmission line effects, frequency dependence of circuit elements, and electromagnetic coupling
    - Correct backannotation dramatically increases the number of elements in circuit simulations causing unusable simulation run times
    - Only a limited number of parasitics are typically added in an ad hoc manner to obtain reasonable run times

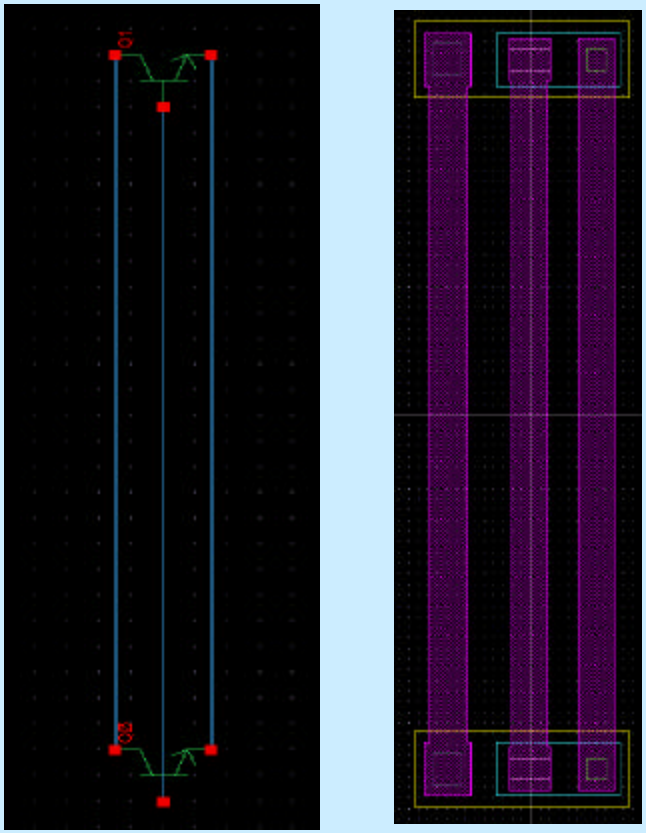
Return

Limitation of current simulations

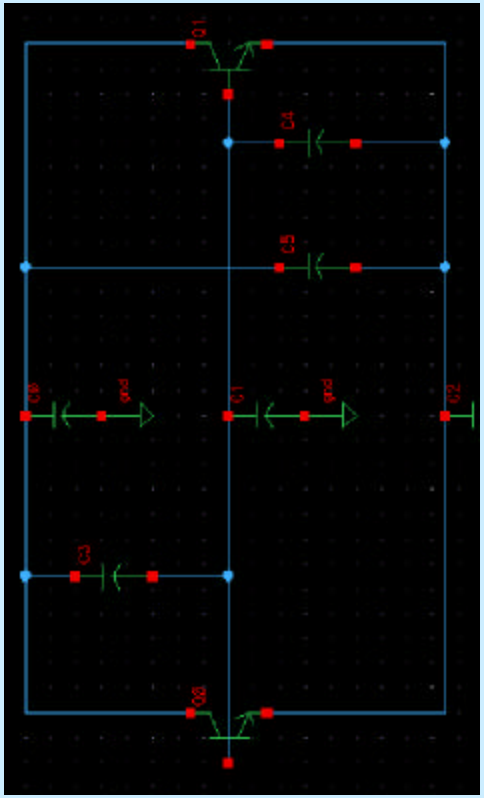
- Transistor models are not always accurate
  - model equations to not fit real devices
  - transistor saturation and breakdown effect not modeled
  - harmonic distortion and non linear effects are not accurate
- Transient analysis is necessary for ADCs, DACs,PLLs, and DDS requiring long simulation
  - 200K points to 50 Meg points to obtain the necessary frequency resolution in an FFT
  - stresses CPU time and available memory
- Thermal noise is not modeled in the large signal transient simulation
  - Large signal behavior of the thermal noise is different then small signal
  - 1/f noise up-conversion into phase noise is not modeled
- Parasitic backannotation
  - Current tools are not adequate for high speed
  - At high speed need a full LRC extraction with coupling
    - Increases number of circuit elements by 10 fold

Return

Backanotation Example



Two transistor circuit & layout

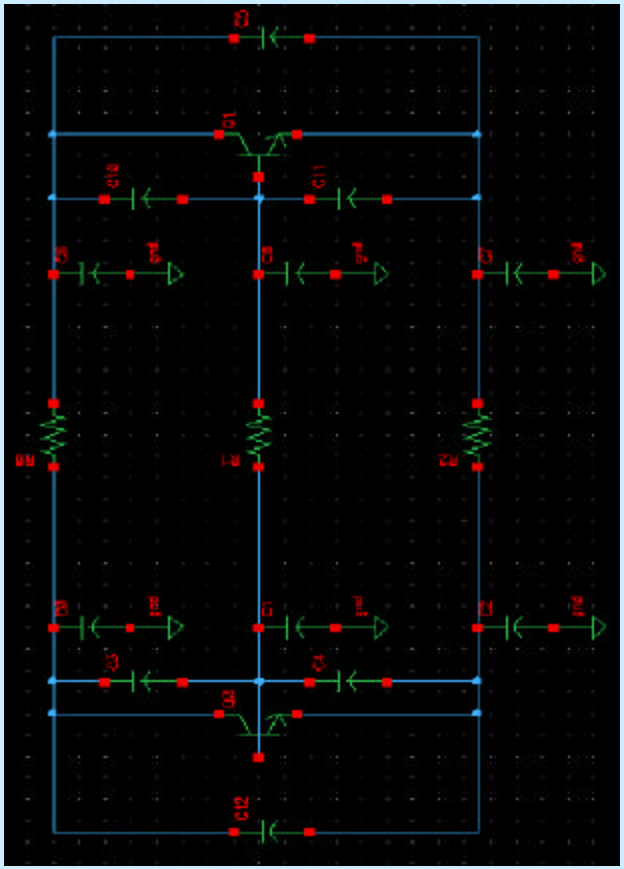


7 devices

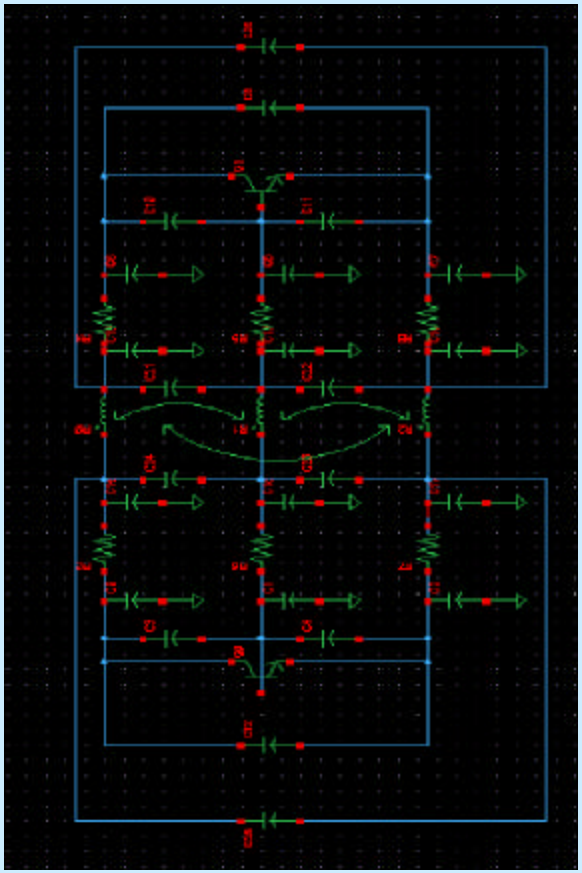
1st Order Extrraction
(Capacitance only)
Valid at only low frequency

Return

Backannotation Example



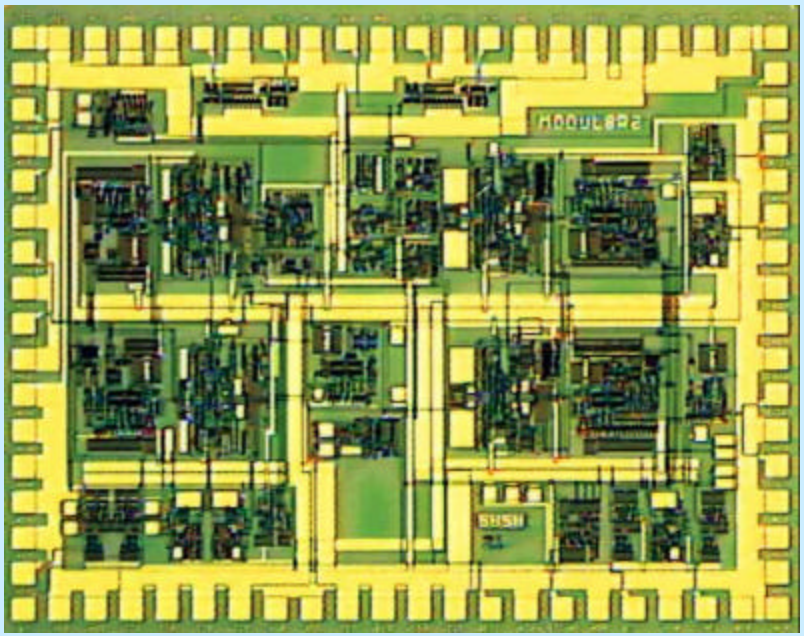
Lumped RC Extraction
17 Devices



Lumped LRC Extraction
35 devices

Return

Backannotation Example



1200 Transistor circuit

Operates at 5 GHz

Capacitive extraction ~ 15,000 devices

Full Lumped LRC extraction ~ 150,000 devices

Lumped extraction good to 5-10 GHz
10-50 GHz need high order filters(3rd order)
50-100 GHz need 3d extraction (radiation not negligible)

Return

What is needed for Mixed Signal CAD

- Need an open frame work that easily integrates multi-vendor tools
- Need better tools and interfaces
  - Top level behavioral description
  - Block level synthesis
  - Layout generation
  - Back annotation of parasitics
  - Circuit Simulation
- Need to improve transient circuit simulation times by orders of magnitude for full transistor level verification
  - Faster CPU's
  - Improved circuit simulation algorithms
- Tools need to be available at a reasonable cost

Return

Mixed-Signal CAD
A View from the Industry

Lawrence Arledge	**Program Manager *, Design**
Jim Hutchby	**Director, Nanostructures and Integration**
Justin Harlow	**Director, Integrated Circuits and Systems**
William Joyner	**Director, CAD and Test**
W. Dale Edwards	**Program Manager, Design**
Ralph Cavin	**Vice President, Research Operations**

Semiconductor Research Corporation

Research Triangle Park, NC

* Mixed Signal Products,
Texas Instruments, Dallas, TX

Return

Acknowledgements

- We acknowledge the helpful technical discussions and contributions of
  - David Yeh, Texas Instruments
  - Felicia James, Texas Instruments

Who is SRC?

- Semiconductor Research Corporation, Research Triangle Park, NC
- SIA-founded private industry consortium which aims to
  - conduct advanced microelectronics research in university community
  - assist in development and sustenance of microelectronics academic infrastructure
  - graduate student support and mentoring
- SRC presently composed of two research programs (*i.e.*, two research models)
  - Core program (industry directed)
  - Focus center research program (university directed)
- Many SRC member companies participated in the Mixed-Signal Task Force described next ...

Return

SRC Mixed-Signal Task Force

- Representatives from twelve SRC member companies developed a needs statement for mixed-signal IC's
- Led by Jim Hutchby and Justin Harlow of SRC
- Not all items are research. Some near-term development.
- Document completed: September 2000

Participating Companies

- AMD
- Cadence
- Conexant
- IBM
- Intel
- Intersil
- Lucent
- LSI Logic
- Motorola
- National Semiconductor
- Texas Instruments
- Semiconductor Research Corporation

Return

Many opportunities in MS (SoC) systems

- Unprecedented ability to use analog and digital on the same chip
- Unprecedented range of applications
- Commercial products moving ahead at very rapid pace
- Cost and time-to-market (TTM) have emerged as key distinguishing items

- … but, saddled with inadequate CAD hierarchy to meet emerging technology capabilities ...

Return

Characteristics of the SoC era

- Up to now, processor and DRAM were drivers
  - CAD hierarchy built up around digital design
  - Designer not need to be EE. Many computer folks.
  - Pricing was quasi-independent of cost (processor)
  - Ultimate needs from technology: speed, transistor count
  - Moore's Law dominant
  - Product lifetimes followed Moore's Law
- SoC era
  - Very price sensitive
  - Short product lifetimes, so TTM crucial
  - Wide diversity of architectures, applications
  - Must reach design maturity quickly, with small team

Return

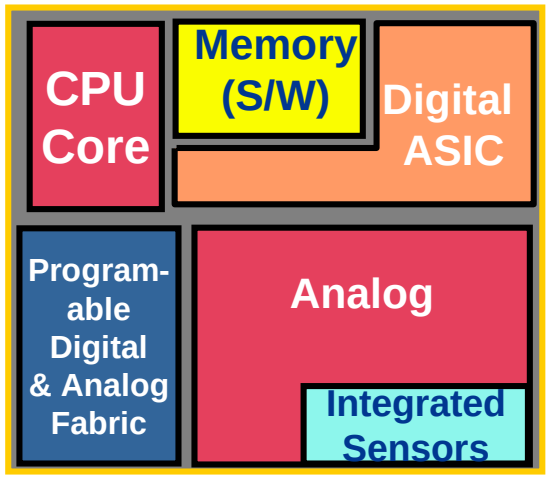
Integrated system trends

Just Yesterday

- "System" = "Big Chip"

- Homogeneous design style
- Synchronous clocking
- Custom, gate-level designs
- Power and I/Os manageable
- Limited embedded software

Now and Later



- True integrated systems
  - Refined system architecture
  - Formal communication protocols
  - Embedded software
  - Memory hierarchies
- Design diversity + >10^9 xtrs + SW
- Asynch or packet-like clock
- IP cores. Re-use of busses.
- Power and I/Os potential problems
- Software reconfigurable systems

Return

How much difference does architecture make? Can CAD get me there?

From ISSCC 1998:

- IBM "Copper Chip" PowerPC
  - Similar to PowerPC 750, 32-bit
  - 480 MHz in IBM CMOS7S
  - *Four more technology generations* to achieve 995 MHz, assuming 1.2X improvement per generation !

Source: IBM

- IBM Austin Research Lab "guTS" prototype
  - Integer subset of 64-bit PowerPC
  - 1.0 GHz in IBM CMOS6X !

Today

- Performance directly proportional to technology capability
  - i.e., 2X better technology produces 2X performance improvement

Future

- System performance from algorithms, architectures, and technology
  - Technology gains usually do not affect system proportionally
  - Algorithms & architectures provide enormous leverage

Return

System architecture can matter more than any other single factor

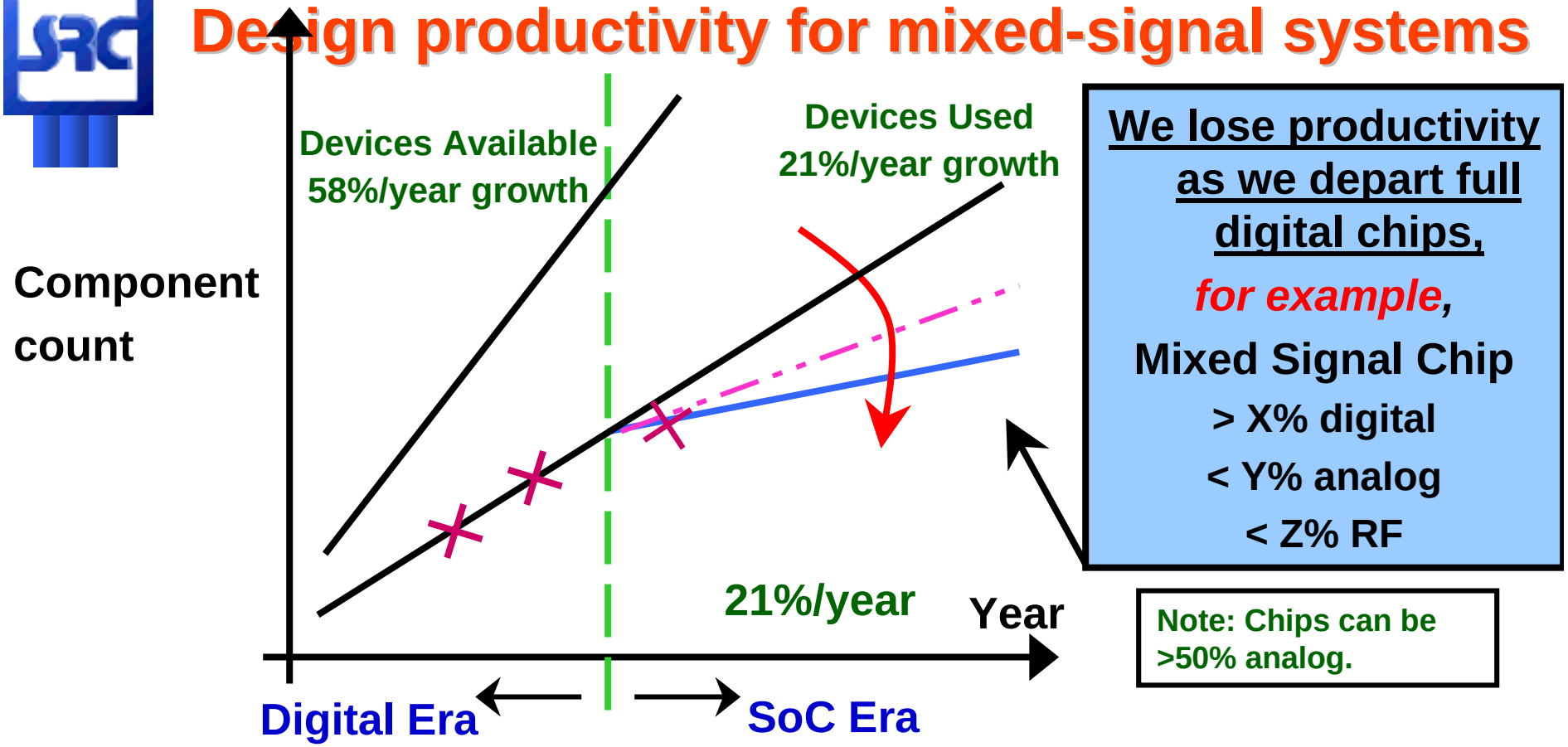
"Not much performance left in the architecture?"

… Look what Transmeta did …

- **Press reports claimed the Crusoe processor**
  - **runs the same applications as other x86 processors**
  - **at one-third to one-thirtieth the power**
  - **while running *at full speed***
  - **and sharing none of the hardware -- in fact, using only one-quarter the transistors**
- **Complete re-thinking of the processor architectures**
  - **software emulation of instructions *vs.* hardware**
  - **innovations in VLIW architectures**
  - **novel use of registers**

Return

Design productivity for mixed-signal systems



- Straight line, but can't "climb the constant slope" with tools made once for all. Much innovation required to jump from point to point.
- Design productivity curve for SoC flattens out dramatically due to complexity of AMS/RF design
- AMS/RF typically has "many more" design spins than digital

Return

What will a design team look like?

- ITRS 2000 indicates
  - design team for core-based ASIC asymptotically approaches
    - 50 people
    - 9 months
    - >200K transistors/designer/month
- This was conceived for a pure digital system.
- It's a stretch to imagine a MS system could be done within these constraints.

Return

“ASIC-ization” of mixed-signal design

- Textured blocks indicate “manual”, but that is relative … many manual steps exist in so-called “automated blocks”
- Data abstraction not sufficiently continuous (esp., from digital to analog sides)
- Making analog keep up with digital design flow is sort of like dragging your pet turtle on a marathon run … it takes time and effort … and you may not win

Digital

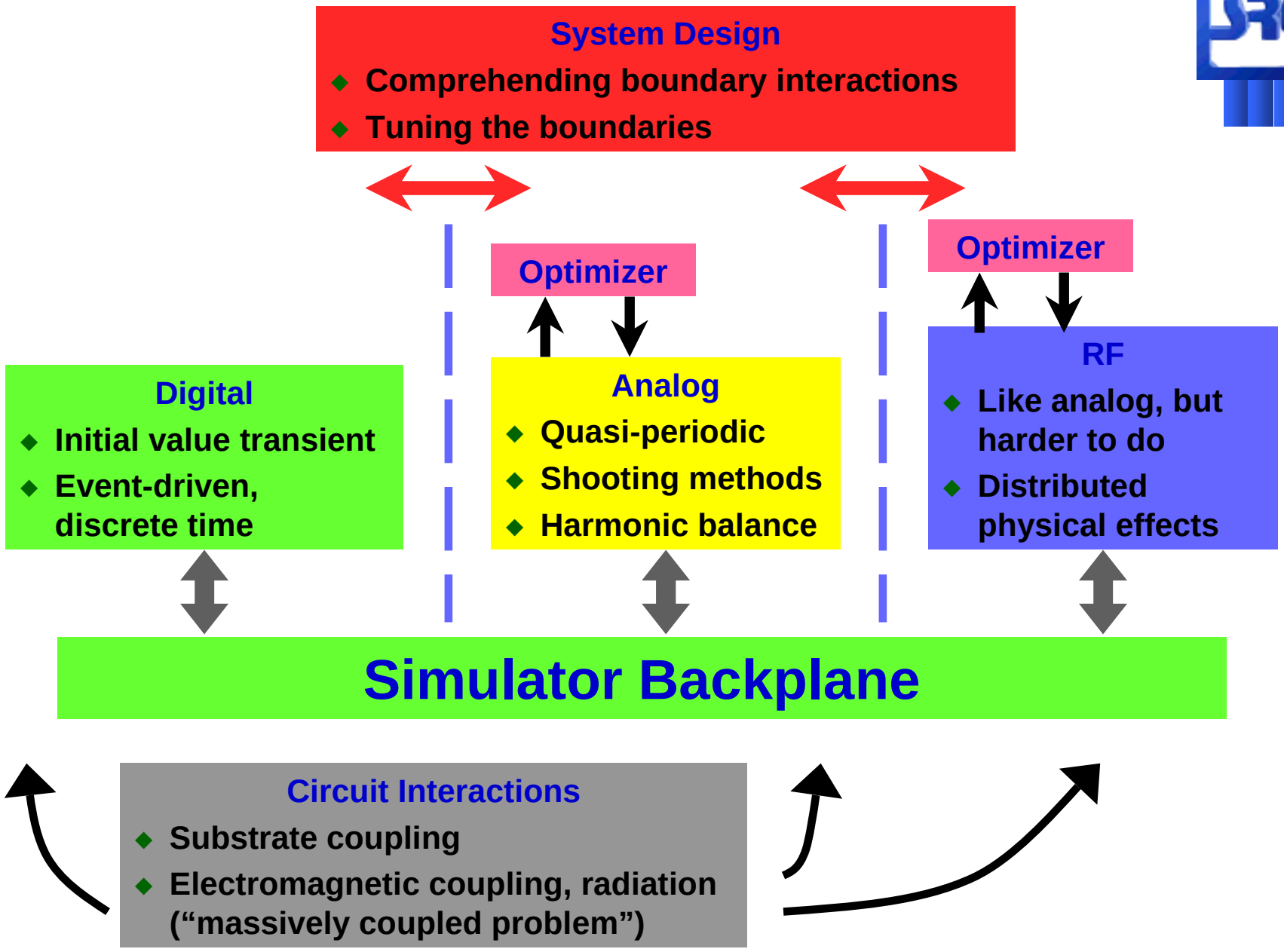
- Behavioral spec
- Verilog, VHDL
- Synthesis
- Physical Design
- Parasitic Extraction
- Verification
- Mask + Fabrication
- Test

Analog

- Behavioral spec
- System modeling
- Circuit topology
- Simulation/ Optimization
- Layout
- Parasitic Extraction
- Verification
- Mask + Fabrication
- Test

Return

E.g., mixed-signal circuit simulation



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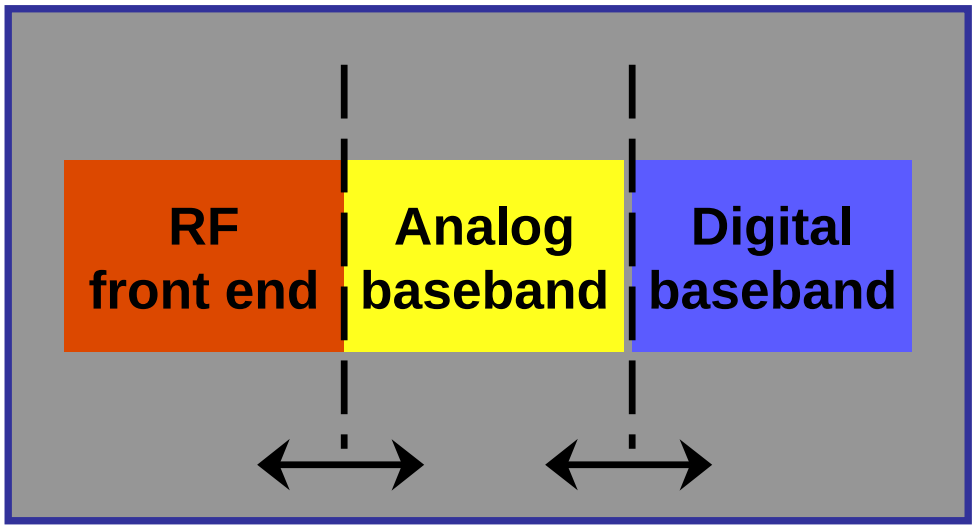
Conceptual Picture of What We Want: Circuits and Systems (CAS) architecture exploration via CAD

- Where are the boundaries? SoC? SoP?
  - Physical barriers
  - System choices, *e.g.*, programmability, ...
  - Cost implications
  - Time to market



- What is the CAS architecture for a particular technology?
- How much in RF? Analog? Digital?
- At each new technology generation: Re-target? Or, re-synthesize?
- Want to “turn dials” to reach optimal system, accounting for cost …

Return

The CAD needs are many

System-level capabilities

- AMS/RF performance inherently tied to devices, wires, physical organization, … ever-changing landscape …
- need for MS architecture exploration and optimization tools to make many choices
  - system partitioning (including SW, A, D, RF, …)
  - coupling to hardware/software co-design … even co-design of HW + SW + package
- synthesis from system-level behavioral specification
- insufficient awareness of physical details important to analog/RF (*e.g.*, substrate coupling, field coupling, …)
- no loop closure from behavioral level to transistor level
- no capability to model consequences of design choices on cost or time-to-market
- yet, the tools are in their infancy

Return

… here are more …

Transistor-level, statistically-based design tools

- Aims of this area
  - design
  - design centering
  - yield analysis
  - performance optimization
  - reconcile the divergent needs of analog and digital w.r.t. manufacturing variations, aid to synthesis
- Tools must be able to search or invent new circuit topologies to meet targets
- Management of parasitics, including explicit accounting for substrate coupling
- Good device models
  - passive devices
  - variable complexity transistor models (D, A, RF)
  - MEMS will be very important in leading edge SoC too

Return

… and these CAD tools too …

Behavioral models

- want circuit and data abstractions to “zoom” at will from compact abstractions to fully detailed descriptions
  - should be able to look at every level of abstraction desired at each point in design hierarchy
  - fully accurate models

Verification tools

- completely different animals for analog than for digital
- some validation of schematic to layout exists now, but other aspects of hierarchy nonexistent -- either as tools or methodologies
- physical, functional, timing

Return

… and still more …

Noise models and simulation

- no method at present to simulate the noise from input to output of system
- need general methods for representation and explicit inclusion of noise throughout design process
- not merely modeling problem … must analyze and extract noise from physical layout … models for simulation
  - inductance
  - substrate coupling … from adjacent or remote circuit blocks … very dependent on particular circuit activity in aggressor and victim blocks
  - crosstalk & radiation/reception (the “massively-coupled problem”)
- *E.g.*, noise macromodeling of digital nets, EMI, ground paths, …

Return

… and the list goes on …

Combined top-down & bottom-up (TDBU) mixed-signal design methodology

- propagation of design constraints
- automatic validation of specifications
- must address possible shortcomings of design languages as they pertain to AMS
- TDBU will not be as “formulaic” for analog/RF as for digital … many intermediate problems to solve … must have access to intermediate abstractions for diagnosis, tweaking, re-design, …
- Design methodology founded on assembly of lower level cores
  - robust simulation needed
  - system level integration is a big hurdle for many reasons, *e.g.*, (substrate noise, timing, power, EMI,

Return

Need for physical CAD continues to grow ...

- Deep submicron (DSM)
  - explosion of data.
  - everything closer together and interacting
  - parasitics important
  - dynamic range (linear) of devices decreased, implying more spectral content
- Design tools must handle all this data … or abstract it in a way that does not invoke unwarranted approximation

Return

The insular areas: test, reliability, packaging

- research is very limited at present in all these areas, that is, w.r.t. AMS/RF
- no systematic methodology exists for robust testing
  - far behind digital in maturity
- reliability presumes commercial needs, not defense care abouts
- packaging must be treated as part of the design problem

Return

And many considerations that have CAD implications

- CAD is not merely design automation, but much more … design space exploration, optimization … provides ability for design creativity
- Key point: higher levels of design (based on cores) implies more physical simulation, not less
- The old CAD infrastructure aimed for processors. We are in infancy in mixed-signal CAD. Need for much research to handle presently-intractable design problems.
- Traditional EE graduates declining … fewer and fewer in population who have background for second-order effects, EM fields, circuit diversity, noise …
- In a large sense, future CAD must do more to make up the gap between designer expertise and design … and tools must break gracefully, since engineer is less capable to fix them.

Return

Imagining the future for defense electronics

- Mixed-signal CAD goes to the heart of communications and sensors, both key areas of defense electronics
- While commercial technology is moving at a very fast pace, it occupies very different point in design space
- For defense electronics
  - cost less important than performance, reliability
  - longer product cycle times
  - robustness in hostile settings (radiation, temperature, …)
  - more need for and willingness to employ novel technology (SiGe, III-V, …)
- "COTS" increasingly means assembly of application-specific SoC's using available cores from disparate sources … hopefully with reliable and high performance
- Defense technology leadership is much more pressed to work far out -- and with rapid turnaround -- due to the excellence other nations have in technology

Return

Conclusions

- Many opportunities in SoC
- Process technology moving faster than design technology (design at all levels: device, circuit, system, package)
- Faced with large problems where intuition not enough, efficient design and CAD methodologies do not exist, and brute force methods too severe
- Much research needed to catch up
- Defense needs will be last to be served by commercial CAD vendors, particularly in realm of expensive (high performance) new technologies
- Axiomatic that leading-edge design/technology must be accompanied by leading-edge CAD

Return

Postscript

- SRC strongly supports the DARPA initiative to explore mixed-signal CAD research opportunities
- Much work to be done by
  - universities
  - government labs
  - industry
- SRC has enjoyed a very constructive relationship with DARPA and other federal agencies through the years
- Willing to continue to provide industry input into this mixed-signal CAD initiative
- SRC contacts:
  - Ralph Cavin, VP of Research Operations
  - Jim Hutchby, Director of Nanostructures & Integration
  - Justin Harlow, Director of Integrated Circuits & Systems
  - Bill Joyner, Director of CAD and Test

Return

CAD Tools for Wideband, Mixed-Signal ICs: A Designers' Perspective

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Silicon Wave Corporation
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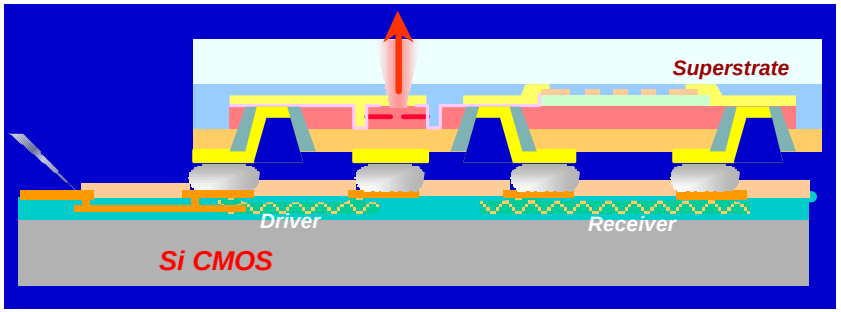
Outline

- What we design
  - FSOI ASICs
  - Parallel Data Link ASICs
  - High-speed PC boards
- Mixed-Signal CAD Tool Flow
- “Holes” in Mixed Signal Tools

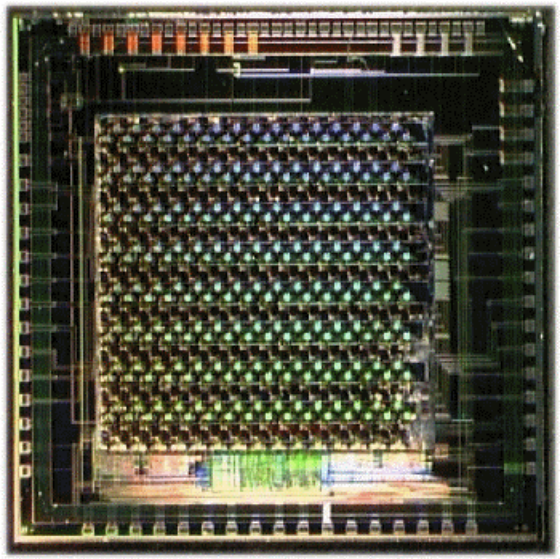
Return

Hybrid Integration of VLSI with 2-D Optoelectronic Device Arrays



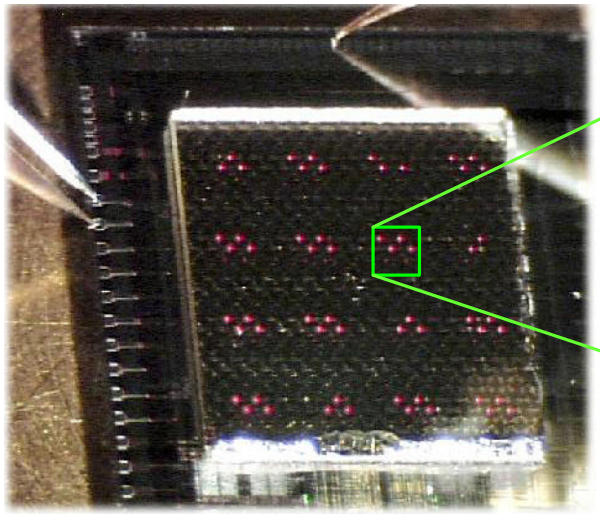
2D OE array bump-bonded directly on top of a Si-CMOS ASIC chip

4 mm

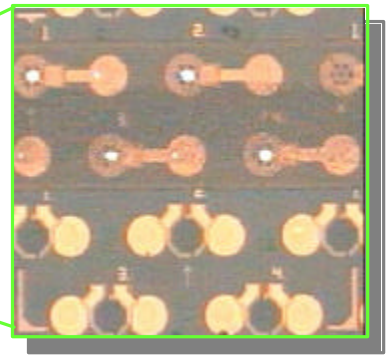


An 256 VCSEL and 256 PD array integrated with a Si-CMOS ASIC.

4x4 clusters (64 VCSELs) powered through the AISC



850nm VCSEL lights are perceived as red on a 3-chip CCD camera.



Four active VCSELs in a unit cell light up, captured by a single-chip CCD camera.

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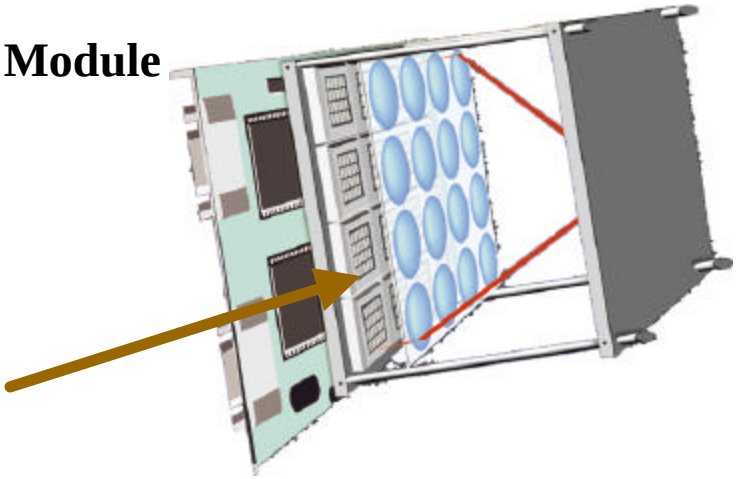
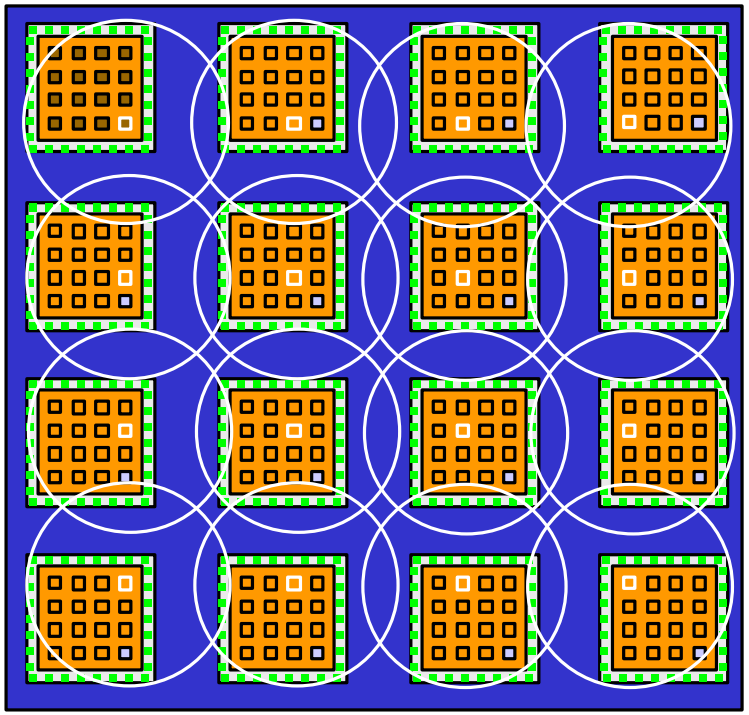
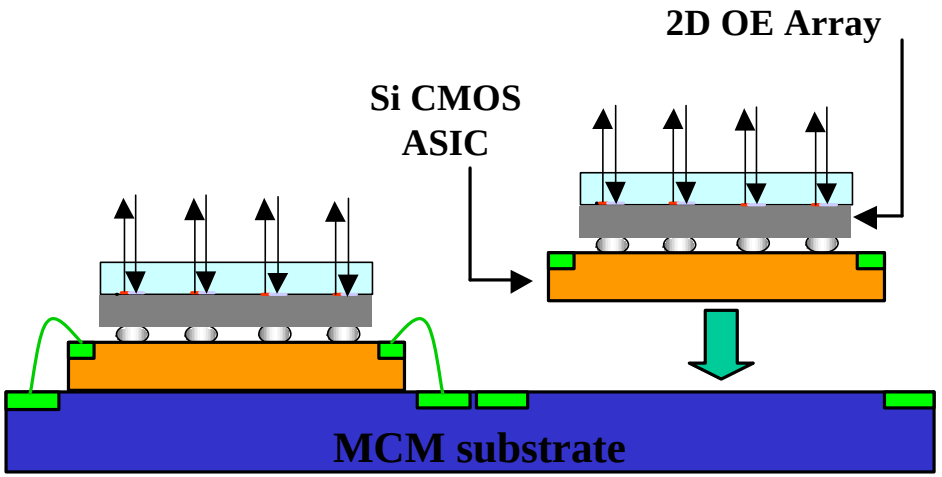
FSOI: Free-Space Optical Interconnects

Switch Module



MCM with 4x4 SPAs





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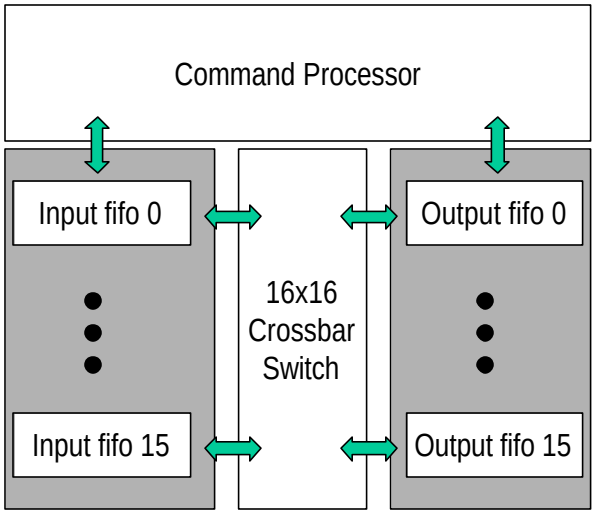
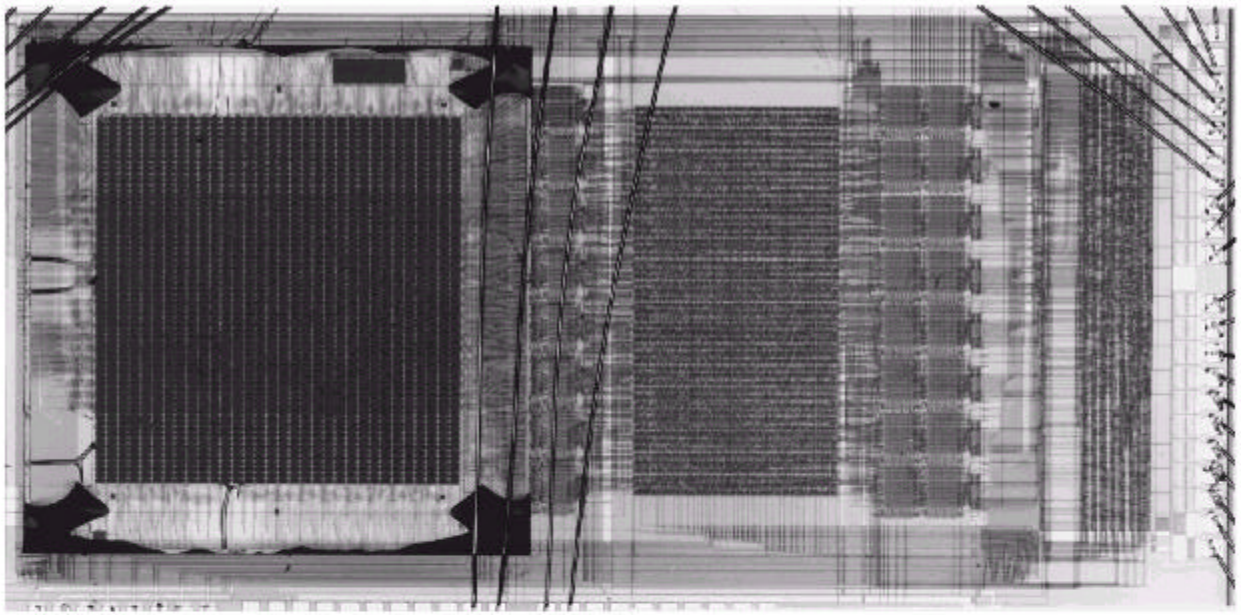
OPTO SWITCH

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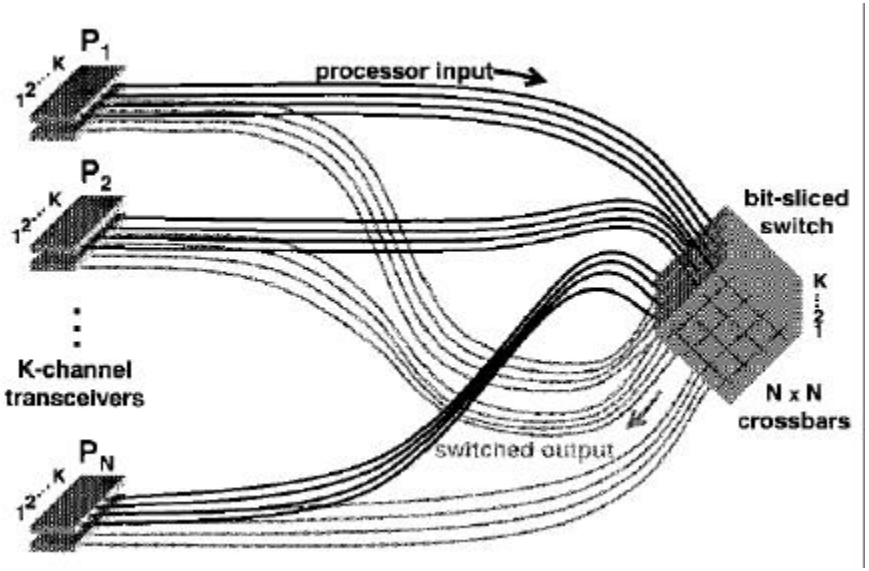

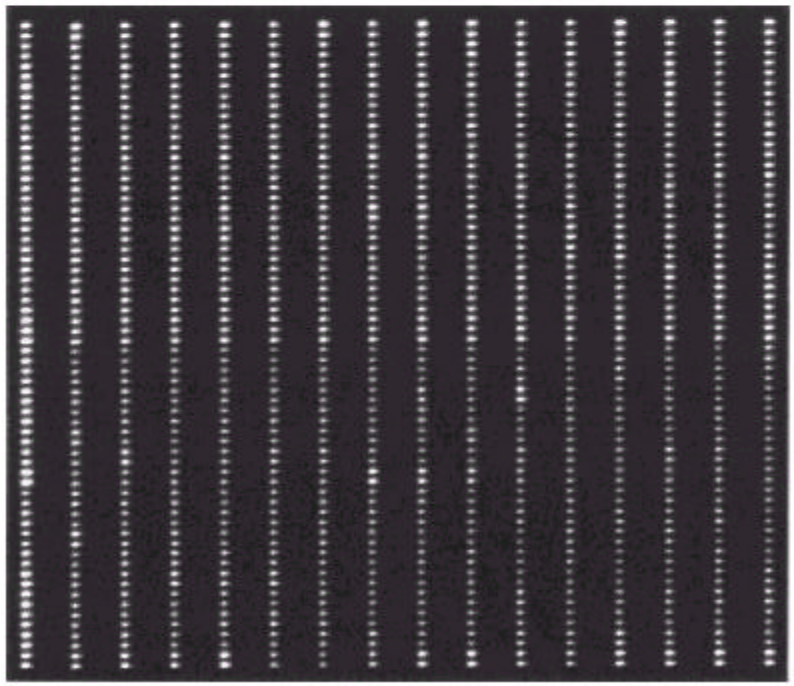

IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, VOL. 5, NO. 2, MARCH/APRIL 1999

Return

FSOI Potential

IBM Unleashes 2.5B Transistor Mainframe

Big Blue hasn't reinvented the wheel recently, instead claiming today to have reinvented the mainframe with its $1 billion, two-year-in-the-making eServer zSeries 900.

The heart of the z900 is the IBM multichip module (MCM). The 5-inch by 5 ¼-inch module contains 35 chips mounted on 101 layers of ceramic glass connected to 4,226 I/O pins by 1 kilometer of wire. The module dissipates 1,200 watts of power and contains 2.5 billion transistors. For more. http://www.electronicnews.com/enews/news/4923-277NewsDetail.asp

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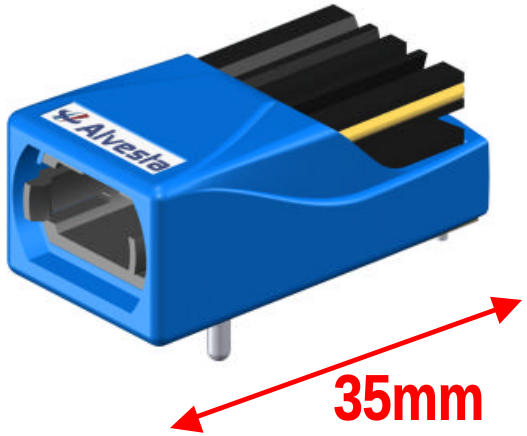
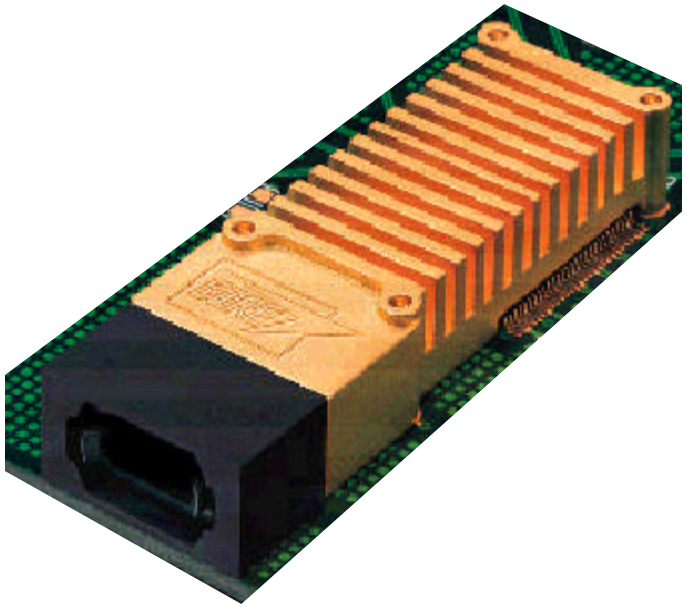
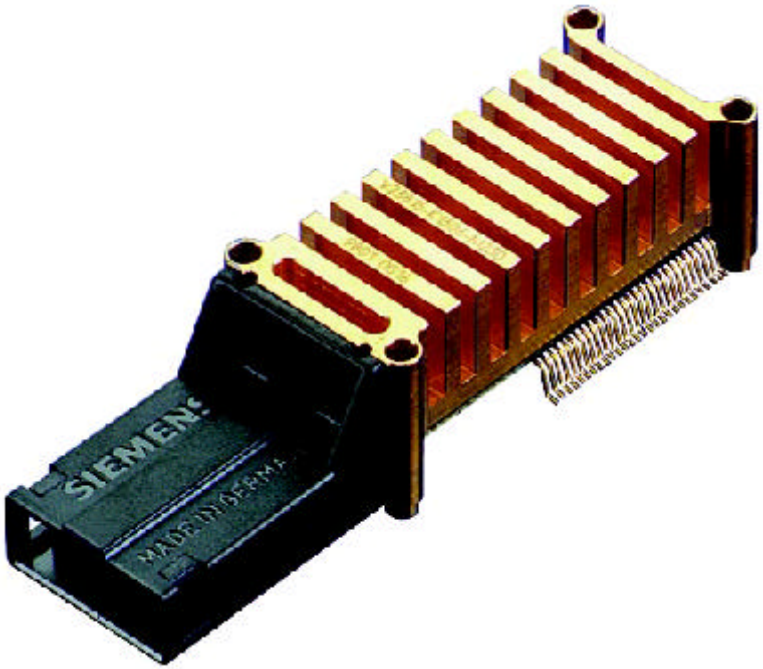
Parallel Optical Data Links







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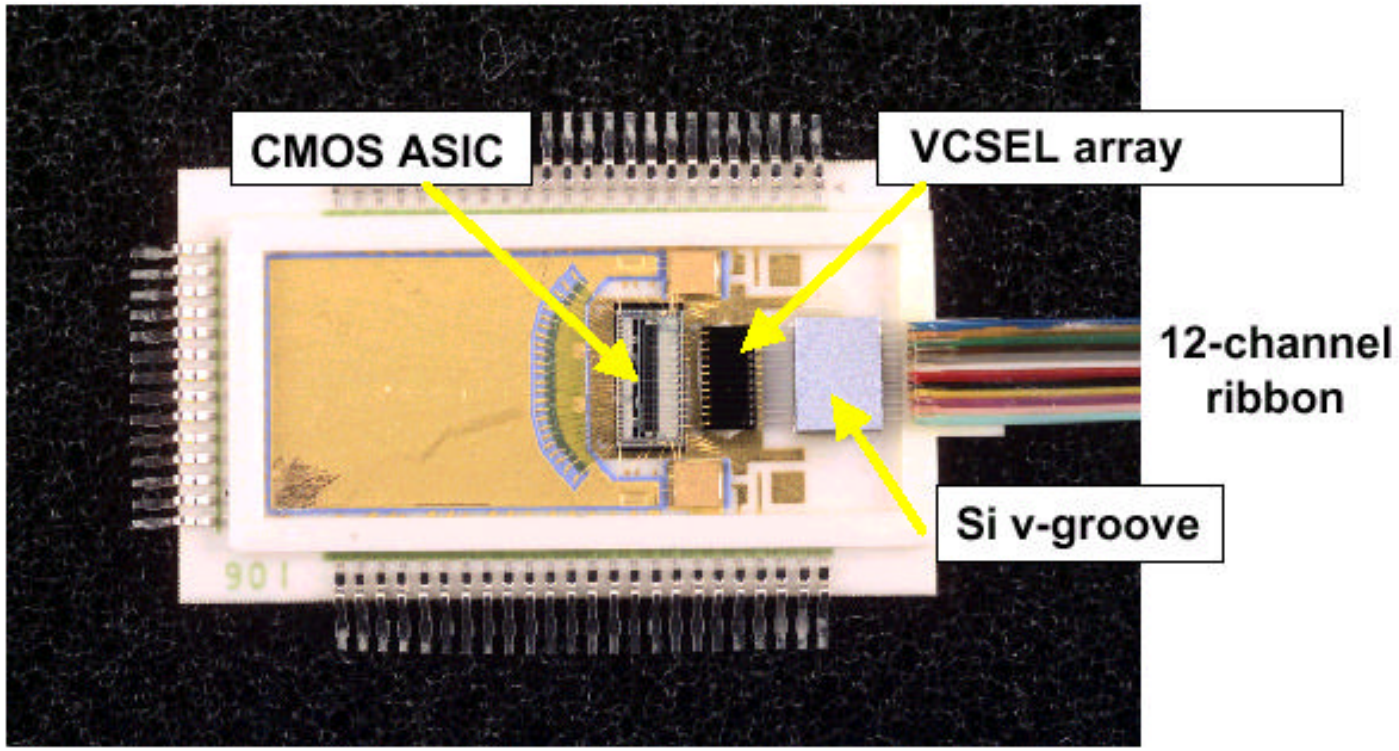
ICs for Parallel Optical Data Links



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12-Gbit Network Interface Card

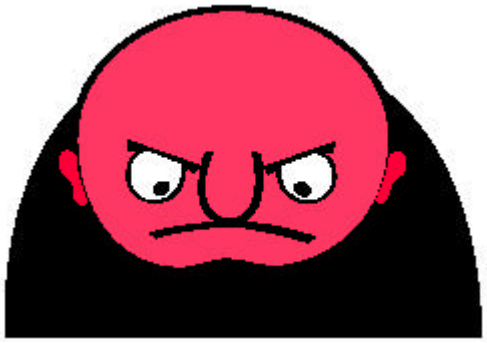
Return

Recent Designs

Function	Asynchronous Data Link	Synchronous Data Link	Crossbar Switch	Optical Packet Router
# Channels	Proprietary	12	25	16
Channel Bit Rate (Gbps)		1.33	2.5	0.8
Aggr. Bit Rate (Gbps)		32	125	26
Optical Interface		24 analog IO @ 1.33GHz	None	640 analog IO @ 50MHz
Electrical Interface		96 TTL IO @ 133MHz	50 LVDS IO @ 2.5GHz	None
Technology		35GHz CMOS	35GHz SiGe	12GHz CMOS
Analog Content		12 Optical TX 12 Optical RX PLL core (IP)	CML logic cells 25 CML IO	320 Optical TX 320 Optical RX
CMOS Digital Content		Standard cells	Standard cells	Standard cells Memory mega-cell
CMOS Digital Function		8B/10B coding SERDES	Configuration logic	Packet Processor Engine
Digital Complexity	10K MOS	50K MOS	1K MOS	100K MOS
Analog Complexity	5K BJT + MOS	5K MOS	10K BJT + MOS	10K MOS

Return

“Real-World” CAD Tool Flow



Design Entry

- Digital - HDL Coding (emacs)
- Analog – Schematic Entry (Composer)

Pre-layout Simulation

- Digital – HDL Simulator
- Analog – Spice
- Mixed Signal – Simulation Backplane (Analog Artist -beta)

Layout

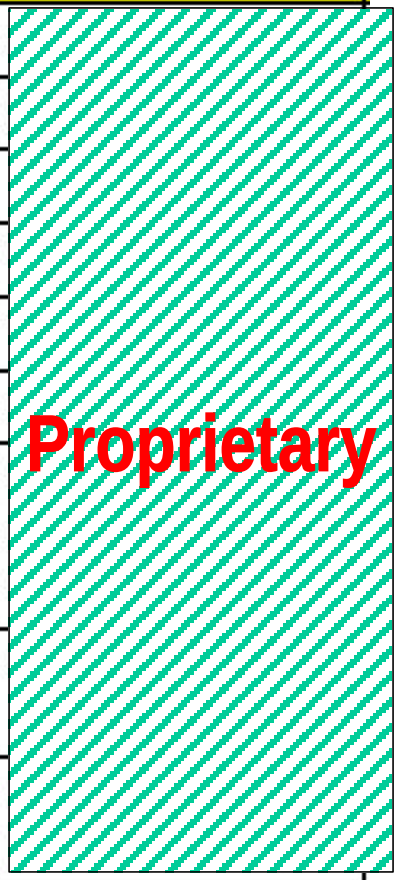
- Digital – Place and Route (Silicon Ensemble)
- Analog – Layout Editor (Virtuoso-XL –new product)

Verification

- DRC, LVS, ERC – Diva
- Extraction – Excalibur (Mentor)
- Full-Chip Simulation – Accelerated Transistor Simulator (ATS -beta)

Full-Chip Simulation Time

Function	Asynchronous Data Link
# Channels	
Channel Bit Rate (Gbps)	
Aggr. Bit Rate (Gbps)	
Optical Interface	
Electrical Interface	
Technology	
Analog Content	
CMOS Digital Content	
CMOS Digital Function	
Digital Complexity	10K MOS
Analog Complexity	5K BJT + MOS



Simulation

<10 μsec Transient to
- power on chip
- initialize digital core
- transcieve on 36 channels.

Pre-layout simulation (ATS, Hspice)

14K MOSFETs

3K BJTs

Couple hours

Post-layout simulation (ATS)

46K Capacitors

0 Rs (Design Kit bug!)

0 Ls (not supported)

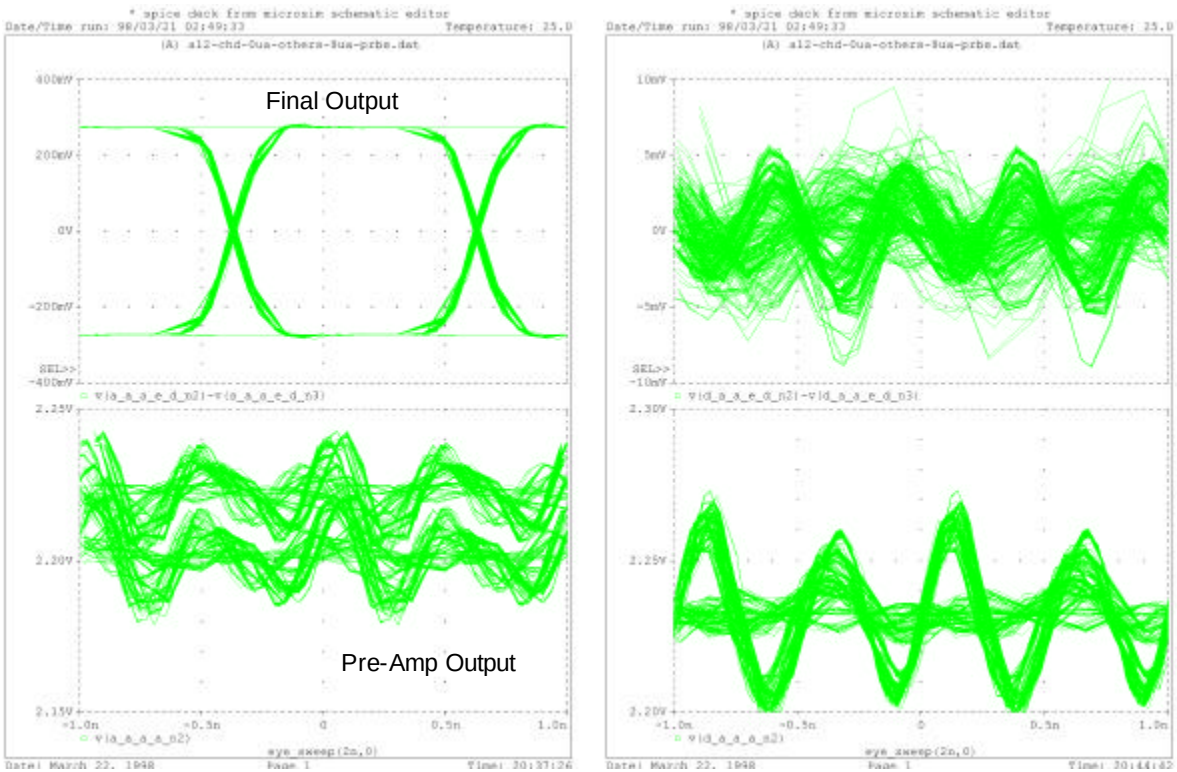
Couple days

Post-layout simulation (Hspice)

No convergence after “cutting out” digital core & ESD diodes

Return

Full Chip Simulation - Data Explosion



Active Channel Quiet Channel

8ua

- Full-chip simulation produces gigabytes of data – how to make sense of it and “trace” for bugs

Return

Models for Interfaces

VCSEL SPICE Model — *Optoelectronics Application*

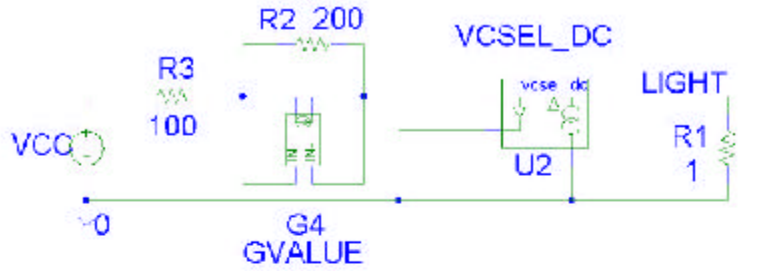


Figure 2 Schematic of circuit used to flatten the power variation over temperature

Design Example

In this section, we describe a simple design case where a negative temperature coefficient (NTC) resistor is used to flatten the power over temperature for a VCSEL. We will look at the nominal cases, as well as a few of the corner cases. NTC resistors do not have linear temperature coefficients, and a series parallel combination of resistors will greatly reduce the non-linearity. The circuit we chose is shown in figure 2. The circuit has a single 5 volt power supply, two resistors, R2 and R3 used to flatten the temperature coefficient, and the NTC resistor. The subcircuit is included as the VCSEL_DC model. The parameter space simulated is summarized in table 1. (NOTE: Values given are for reference only, refer to the data sheets for the actual limits) Figure 3a is a plot of the output power variation as a function of temperature without and with the NTC resistor, respectively, for the worst cases of increasing and decreasing power described in Table 1. The output power variation is dramatically decreased with the addition of the NTC resistor. In this case, we used a NTC resistor with R_0=1000 Ω, and β=4100. This is representative of a NTC resistor TBPS1x102x410H5Q from Taiyoyuden products.

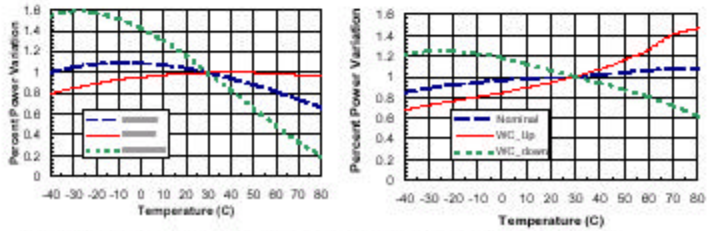
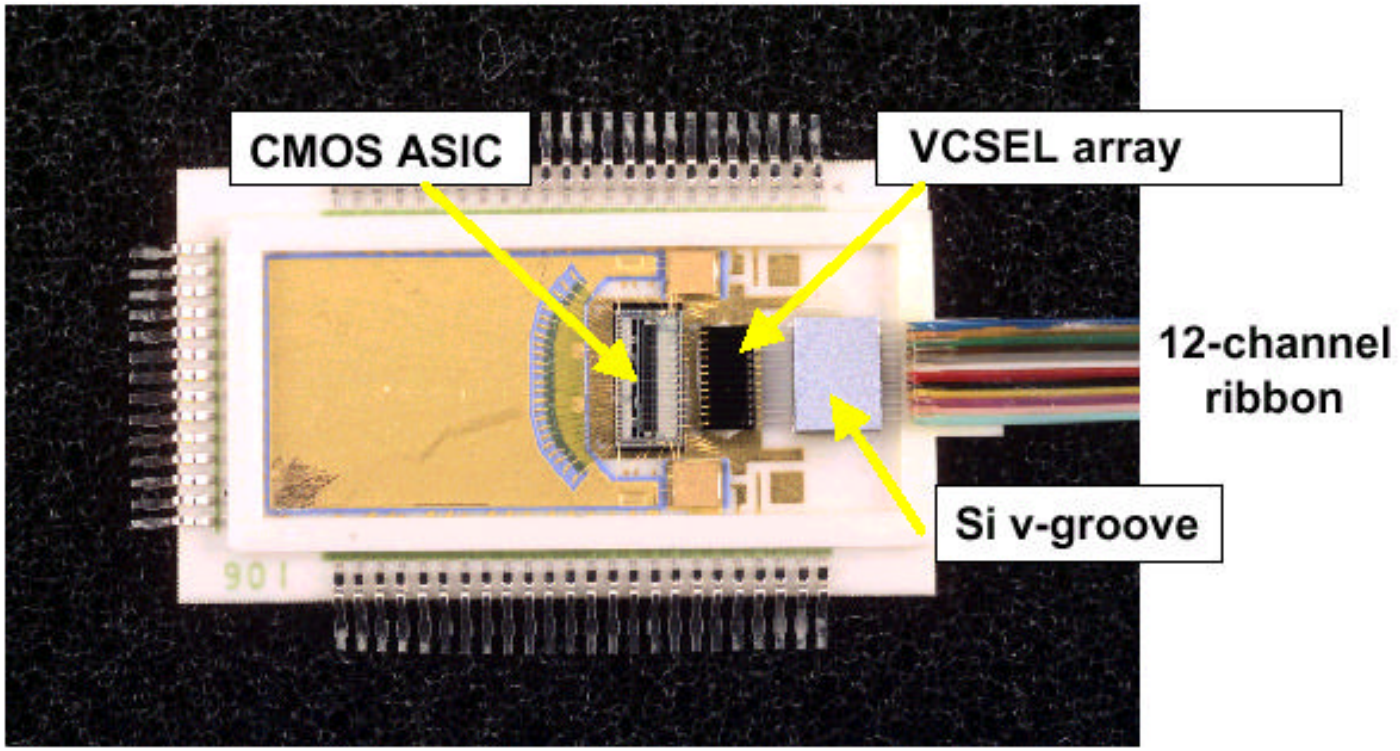


Figure 3 Worst case power variation without thermistor (left) and with thermistor (right)

- At GHz & Ft limits of technology – accurate modeling of optoelectronic devices is a must!

Return

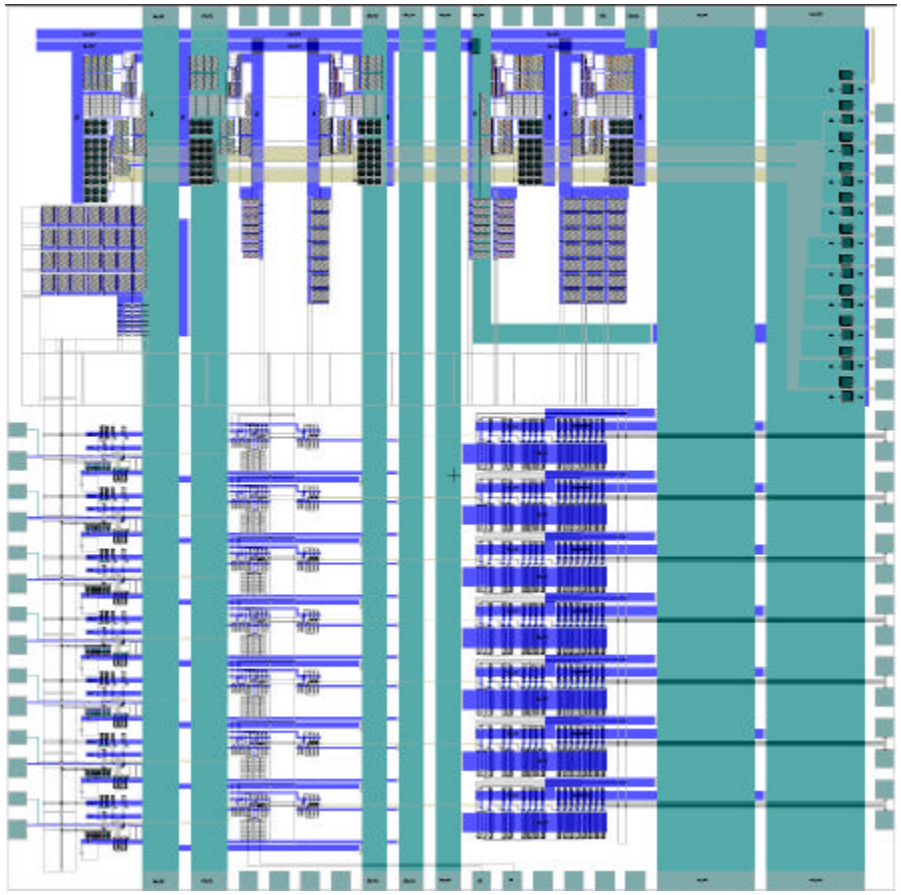
Package & Power Supply Modeling

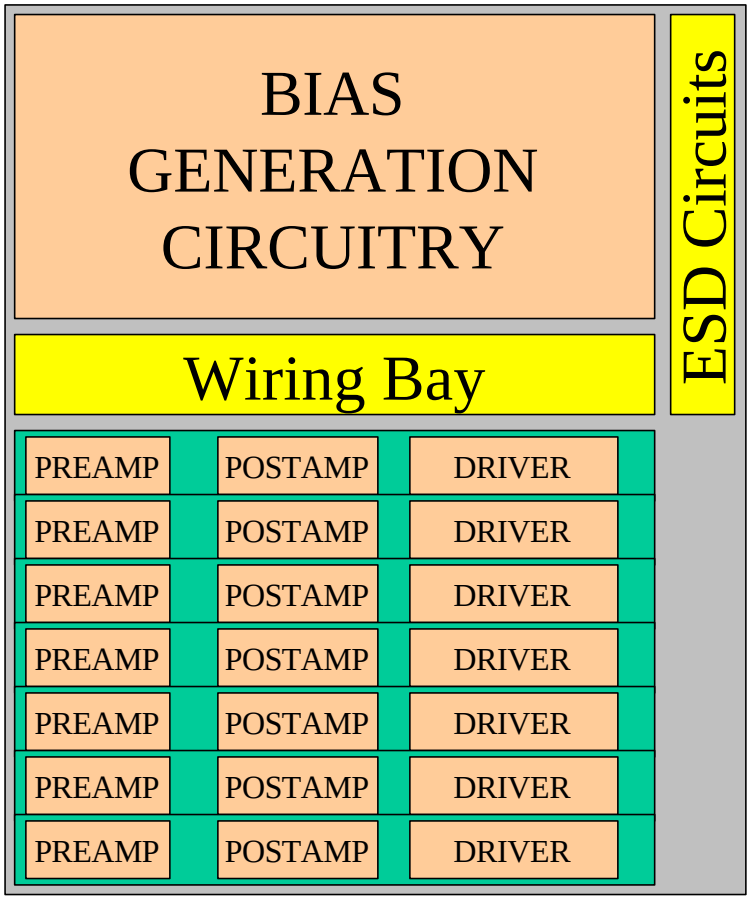


- At GHz & Ft limits of technology – accurate modeling of electrical package & power supply is a must!

Return

Accidental Amplifier Problem





- In mixed-signal designs, complex “quiet” bias circuits and digital section often become oscillators or cause oscillations.

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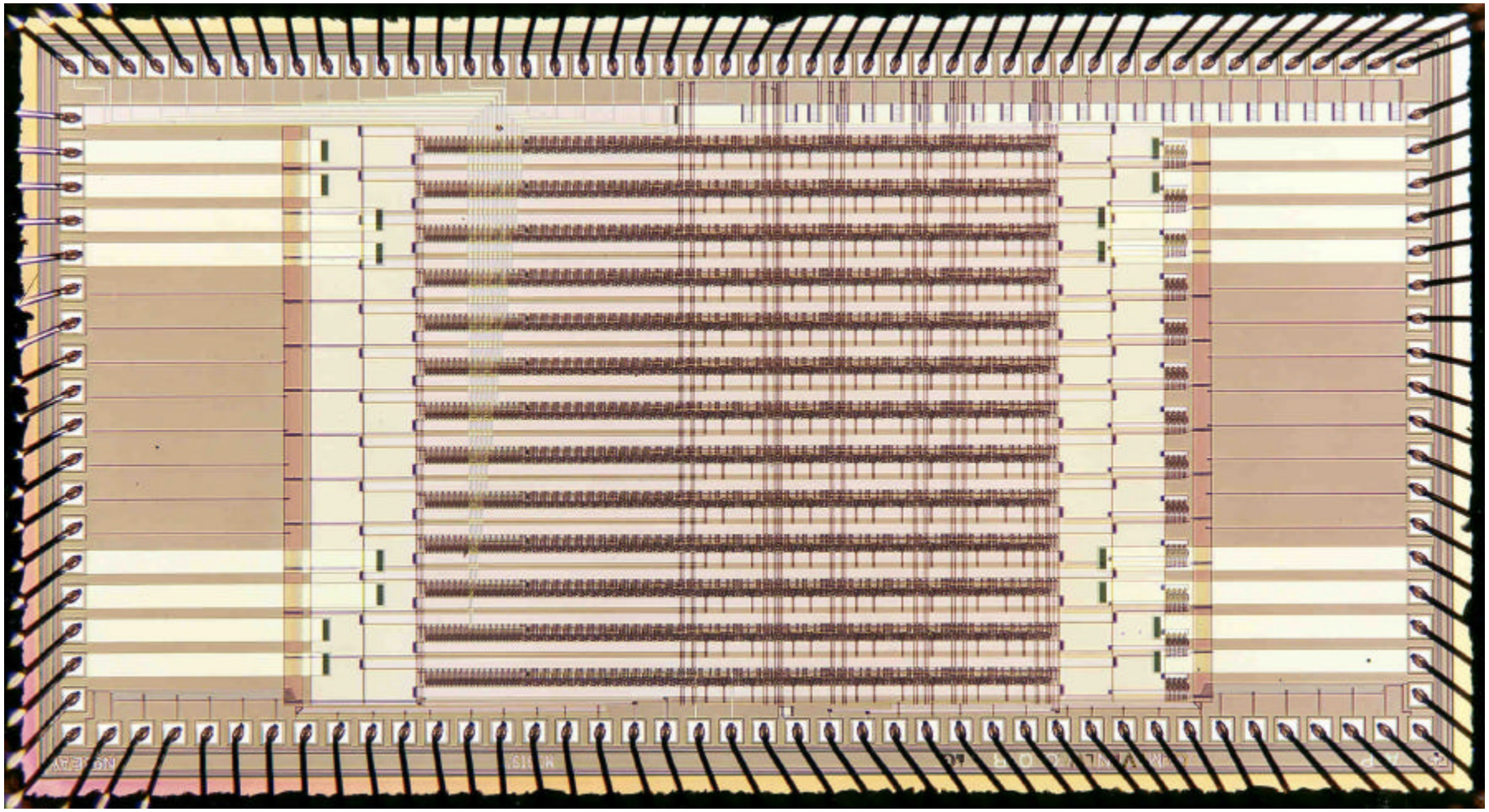
CML Routing Capability



- GHz digital design is going differential CML especially in mixed signal to reduce noise – but no P&R tool, must do full-custom layout.

Return

“Holes” in Mixed Signal Tools

- ~~Full-chip simulation on extracted netlist~~
- Full-chip simulation produces gigabytes of data – how to make sense of it and “trace” for bugs
- Standard models for Optical and Electrical Interfaces
- Modeling power supply noise & crosstalk
- Find accidental amplifiers (oscillation hunter)
- Need P&R tool for CML differential routing
- Support agile clocking and dynamic power supplies

Return

“Holes” in Mixed Signal Tools

- Need standard schematic symbols for analog IP
- Expensive to build mixed-signal design kits
- Encrypted design kits and IP cores are problematic
- Hard to find analog cell libraries & analog IP
- How to migrate designs between technologies
- Standard methodology for simulating process variations
- Links to system level simulation
- Tool integration and design management are not simple
- Area pad router for hybrid OEIC

Return

Automated design of integrated circuits with area-distributed input–output pads

Richard Rozier, Ray Farbarik, Fouad Kiamilev, Jeremy Ekman, Premanand Chandramani, Ashok V. Krishnamoorthy, and Richard Oettel

We present a method for automating the creation of complementary-metal-oxide-semiconductor (CMOS) integrated circuits that successfully utilizes a large number of area-distributed pads for input–output communication. This method uses Duet Technologies' EPOCH computer-aided-design tool for automated placement and routing of CMOS circuitry, given a schematic netlist as an input. The novelty of this approach is that it uses Duet Technologies' EGGO program to place and route area-pad signals. To verify this methodology, it is applied to the design of a digital signal-processing circuit, with 200 optical area-pad input–outputs and 44 perimeter-pad input–outputs, that is being fabricated with Bell Labs 1997 CMOS–multiple-quantum-well foundry. The layout results are as good as or better than the results obtained by manual layout.

OCIS codes: 200.2610, 200.4650, 250.5300.

1. Introduction

Recent developments in the silicon complementary-metal-oxide-semiconductor (CMOS) integrated-circuit (IC) industry have focused heavily on packaging and interconnect technology. Multichip module (MCM) designs, such as the Intel Pentium-Pro, have been explored. A large amount of research has been done to develop free-space optical interconnects (FSOI's): IC's that have light-producing and -detecting devices attached to them. These devices establish data communication by use of light-refractive, -diffractive, or -reflective optics.[1,2] Both MCM's and FSOI's utilize area-distributed input–output (I/O) pads on the surface of the IC die that attach through flip-chip bonding to other substrates or devices. Area pads are a natural evolution in the way that IC's are packaged and communicate with each other. When the I/O connections are distributed over the surface area of the IC rather than just the perimeter, the number of I/O's increases from $4s$ to As^2, where s is the number of I/O's that can fit on one side of the die and A ($A > 1$) is a scaling factor that accounts for the reduction in the pitch of area-distributed pads versus perimeter pads. Designs with as many as 2000 I/O's are being produced.[3] In addition, designs with area-pad I/O's have higher performance because the chip-to-chip connection is made through low-capacitance metal traces[4] (MCM's) or optical devices[5] (FSOI's). Thus the trend for future implementations of digital IC systems is to use IC's with area-pad I/O's.

In the past placement and routing of the core circuitry had to be performed independently of placement and routing of the area pads. One means of accomplishing this task was to perform a layout of the core and then to route the core to the ports along the perimeter of the chip. After this was done, the designer created an area-pad mask in the top layer of metal. This mask included all area pads as well as the hand-drawn routing of the signals from the area pads to fixed-location ports that matched the locations of the ports for the core circuitry. The final step was to place and align the area-pad mask over the core circuitry. There is great room for human error in this method.

VLSI computer-aided-design (CAD) tools have evolved to automate some of these details a little bit better. Several CAD tool suites offer extensive CMOS transistor layout and analysis programs.

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Received 9 December 1997; revised manuscript received 30 March 1998.

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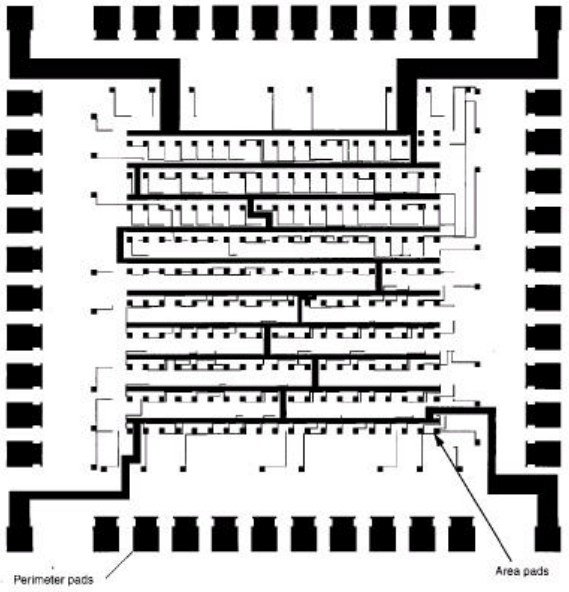

Fig. 13. Multiply–accumulate layout (metal 3 only).

quested amount of power (a function of route width) from the area power pads to the design. This power requirement is determined by the power analysis tool.

A technique called windowing (Fig. 10) is used by the router to isolate selectively a section of the design. This enables the power pads to be routed independently, avoiding power-pad interconnection. In this manner power pads are isolated and can supply power to a window within the design.

The window size and shape affect the performance of the router. Currently, the router simply masks

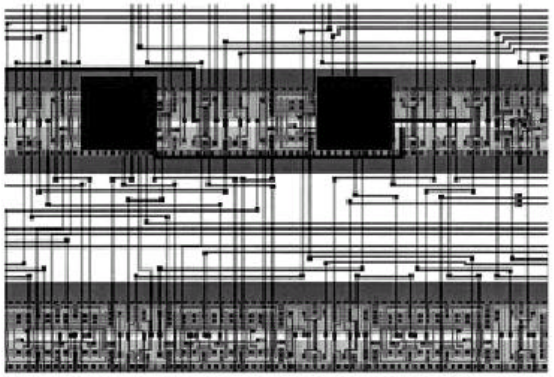

Fig. 14. Layout close-up showing area pad and underlying circuitry.